Interface Traps in Surface-Potential-Based MOSFET Models

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ABSTRACT

Surface or interface properties along the surface channel region have great influences on the MOSFET characteristics. The interface-trap density increases during the repeated program-erase cycling of non-volatile floating-gate and SONOS memory transistors. Thus, the compact modeling community faces great challenges to model the interface-trap effect, which is an important step towards modeling device reliability. In this work, the unified regional surface potential (URSP) approach is extended to explore the effect of interface traps at the SiO_2/Si interface on the surface-potential and gate-capacitance lineshapes in bulk MOSFETs. Due to the trapped charges alone surface channel region, the interface traps significantly distort the surface-potential and gate-capacitance curves. The result suggests that the explicit URSP model has powerful capability to characterize interface-trap properties without major loss of accuracy.

Keywords: Interface traps, compact model, MOSFET, paired-linear traps, unified regional surface potential

1. INTRODUCTION

As MOS transistors become smaller and more highly integrated, device degradation has a great impact on its reliability as a function of the applied voltages over time. Interface-trap density increases during the transistor operation or stress which adversely impacts the device reliability. The generation of interface traps degrades device performance, such as the threshold-voltage shift and drain-current reduction [1], [2]. In this work, we will extend the explicit analytic URSP approach [3], [4] to explore the interface traps on device characteristics for conventional bulk MOSFETs. The exact iterative solution will be included as a reference to benchmark the accuracy of the URSP approach. Based on the perturbation theory at the SiO_2/Si interface [5], a paired-linear distribution of neutral interface traps with linear energy distributions of neutral electron and hole traps will be theoretically studied on device characteristics. Since interface-trap density increases with the increasing of transistor write-erase cycles, investigations will focus on the effect of high concentration of interface traps on device characteristics, especially important in memory transistors after many write-erase cycles, such as those used in the flash memory stick.

2. MODEL FORMULATION

The gate-voltage equation with interface-trap charges is expressed as

$$V_{gb} = \phi_s + \Phi_{MS} - \frac{Q_{IT}}{C_{ox}} + \mathrm{sgn}(\phi_s)\,\Upsilon\sqrt{f_\phi} \tag{1}$$

$$f_\phi = v_{th}\left[\left(e^{\frac{-\phi_s}{v_{th}}} + \frac{\phi_s}{v_{th}} - 1\right) + \left(e^{\frac{\phi_s}{v_{th}}} - \frac{\phi_s}{v_{th}} - 1\right)e^{\frac{-(2\phi_{Fp}+V_{cb})}{v_{th}}}\right]. \tag{2}$$

where Φ_{MS} is the work-function difference between metal and semiconductor, and Q_{IT} is the total interface-trap charge per unit area. The Φ_{MS} equals to the flat-band voltage V_{FB} when the interface-trap charge is zero. $\Upsilon = (2q\varepsilon_{Si}p_0)^{1/2}/C_{ox}$ is the body factor in which $p_0 = n_i\exp(\phi_{Fp}/v_{th})$ is the "remote" majority carrier concentration. Other symbols in (1) have their usual meanings. The $V_{cb} = \phi_{Fn} - \phi_{Fp}$ in (2) is the electron–hole quasi-Fermi potential difference (imref-split) due to the voltage applied between the source and drain terminals. The ϕ_{Fp} is the quasi-Fermi potential of majority carriers given by

$$\phi_{Fp} = v_{th}\ln\left(\sqrt{\left(\frac{N_A - N_D}{2n_i}\right)^2 + e^{\frac{-V_{cb}}{v_{th}}}} + \frac{N_A - N_D}{2n_i}\right) \tag{2a}$$

while the bulk Fermi potential is

$$\phi_F = v_{th}\sinh^{-1}\left(\frac{N_A - N_D}{2n_i}\right) \approx v_{th}\ln\left(\frac{N_A}{n_i}\right) \tag{2b}$$

in which the second approximate equality holds when $N_A >> N_D > n_i$. ϕ_{Fp} in (2a) takes into account of hole transport due to the voltage applied to the drain and source terminals relative to the bulk terminal, which is not fixed to the equilibrium value of ϕ_F in (2b).

The essential device physics of URSP is contained in the regional surface-potential solutions in the respective strong-accumulation, weak-accumulation, depletion, and strong-inversion regions. When the transistor is biased in the strong-accumulation or strong-inversion regions, the net charge is dominated, respectively, by holes and electrons. Without considering interface-trap charges, the implicit (1) in strong accumulation, weak accumulation, depletion and strong inversion regions can be respectively rearranged as

$$V_{gb} = \phi_s + \Phi_{MS} + v_{th}\Upsilon\exp(-\phi_s / v_{th}), \quad \left(V_{gb} << \Phi_{MS}\right) \tag{3a}$$

$$V_{gb} = -\phi_s + \Phi_{MS} + \Upsilon\sqrt{-\phi_s}, \quad \left(V_{gb} < \Phi_{MS}\right) \tag{3b}$$

$$V_{gb} = \phi_s + \Phi_{MS} + \Upsilon\sqrt{\phi_s}, \quad \left(\Phi_{MS} < V_{gb} < V_t\right) \tag{3c}$$

$$V_{gb} = \phi_s + \Phi_{MS} + v_{th}\Upsilon\exp[(-\phi_s - 2\phi_{Fp} - V_{cb})/v_{th}], \left(V_{gb} >> V_t\right) \tag{3d}$$

The surface potential in strong accumulation and strong inversion regions can be solved from the third-order polynomial in (3a) and (3d), while the surface potential in weak accumulation and depletion regions can be computed from the second-order polynomial in (3b) and (3c). In order to obtain smooth transitions from strong-accumulation to weak-accumulation regions and from depletion to strong-inversion regions, two smoothing functions are respectively given by:

$$\vartheta_{eff,cc}\{x, x_{sat}; \delta\} \equiv x_{sat} - 0.5\left[x_{sat} - x + \delta - \sqrt{(x_{sat} - x + \delta)^2 - 4\delta x_{sat}}\right] \tag{4a}$$

$$\vartheta_{eff,ss}\{x, x_{sat}; \delta\} \equiv x_{sat} - 0.5\left[x_{sat} - x - \delta + \sqrt{(x_{sat} - x - \delta)^2 + 4\delta x_{sat}}\right] \tag{4b}$$

Thus, the final single-piece explicit surface potential in the whole region is expressed as

$$\phi_s = \vartheta_{eff,cc}\left\{\phi_{asub}, \phi_{str,cc}; \delta_{cc}\right\} + \vartheta_{eff,ss}\left\{\phi_{sub}, \phi_{str,ss}; \delta_{ss}\right\}. \tag{5}$$

The neutral interface trap is defined as an electrically neutral trapping or binding potential that can bind only one electron or one hole. The charge formulae of the electron traps Q_{ETi} and neutral hole traps Q_{HTi} are given by [6]

$$Q_{ETi} = -qN_{ETi} \times \frac{c_{ns}n_s + e_{ps}}{c_{ns}n_s + e_{ns} + c_{ps}p_s + e_{ps}} \tag{6a}$$

$$Q_{HTi} = qN_{HTi} \times \frac{c_{ps}p_s + e_{ns}}{c_{ns}n_s + e_{ns} + c_{ps}p_s + e_{ps}} \tag{6b}$$

where N_{ETi} and N_{HTi} are the neutral electron-trap and hole-trap densities for the ith energy level, respectively. The total interface-trap density N_{IT} is the sum of the all N_{ETi} and N_{HTi}. c_{ns} and c_{ps} are the electron and hole capture-rate coefficients, e_{ns} and e_{ps} are the electron and hole emission-rate coefficients, and n_s and p_s are the electron and hole surface concentrations given by

$$n_s = n_i \exp[(\phi_s - \phi_{Fn})/v_{th}] \tag{7a}$$

$$p_s = n_i \exp[(\phi_{Fp} - \phi_s)/v_{th}]. \tag{7b}$$

From detailed balance near thermal equilibrium and assuming Boltzmann distribution of electron and hole concentrations, e_{ns} and e_{ps} are given by

$$e_{ns} = c_{ns}n_i \exp(+E_{TI}/kT) \tag{8a}$$

$$e_{ps} = c_{ps}n_i \exp(-E_{TI}/kT) \tag{8b}$$

where E_{TI} is the energy level of interface traps measured from the intrinsic Fermi level E_I. k is the Boltzmann constant, and T is the transistor temperature. According to equations (6)-(8), the total trap charge $Q_{IT} = \sum(Q_{ETi} + Q_{HTi})$ is a function of the surface potential ϕ_s and, hence, applied gate voltage V_{GB} since the amount of interface-trap charges depends on the electron and hole concentrations along the surface-channel region.

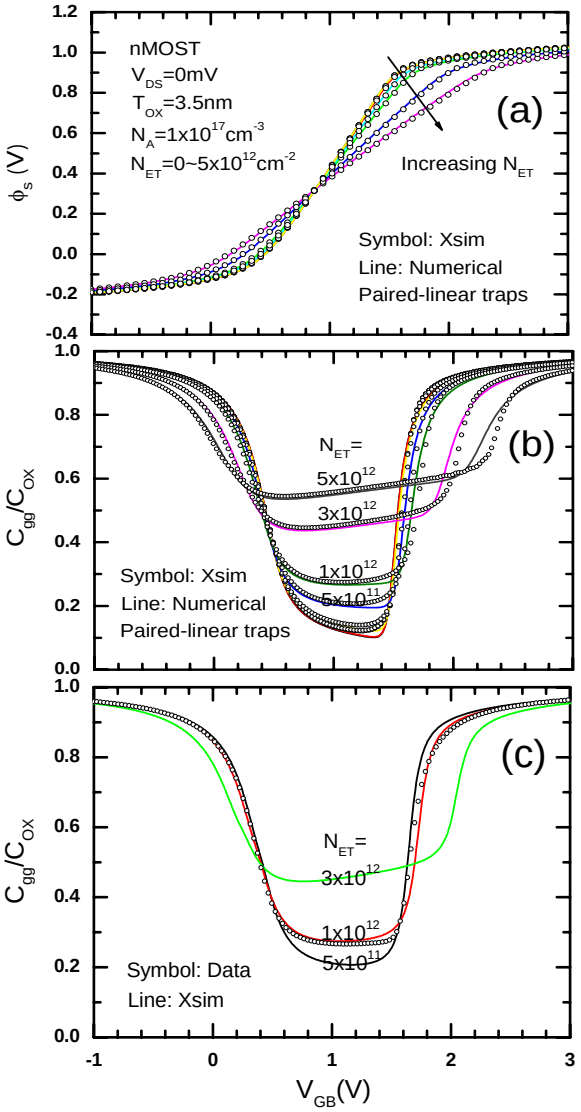

Fig. 1. (a) Effect of interface-trap density on surface-potential lineshape, (b) effect of interface-trap density on normalized C–V curves, and (c) trap-density extraction from C–V curves. N_{ET} = 0, 1.0×10^{10}, 1.0×10^{11}, 5.0×10^{11}, 1.0×10^{12}, 3.0×10^{12}, and 5.0×10^{12} cm^{-2}.

For a three-dimensional bulk model, the ratio of neutral electron traps to neutral hole traps is given by [7]

$$R = \frac{D_{ET0}}{D_{HT0}} = \frac{1.09412}{0.5228205} = 2.095526 \tag{9}$$

where D_{ET0} and D_{HT0} are the densities of states at the conduction- and valence-band edges, respectively. For a linear distribution of interface traps, the total densities of the neutral electron traps N_{ET} and neutral hole traps N_{HT} are respectively given by

$$N_{ET} = \int_0^1 (D_{ET0} \times E)\, dE = \frac{D_{ET0}}{2}, \tag{10a}$$

$$N_{HT} = \int_0^1 D_{HT0} \times (1 - E) dE = \frac{D_{HT0}}{2}. \tag{10b}$$

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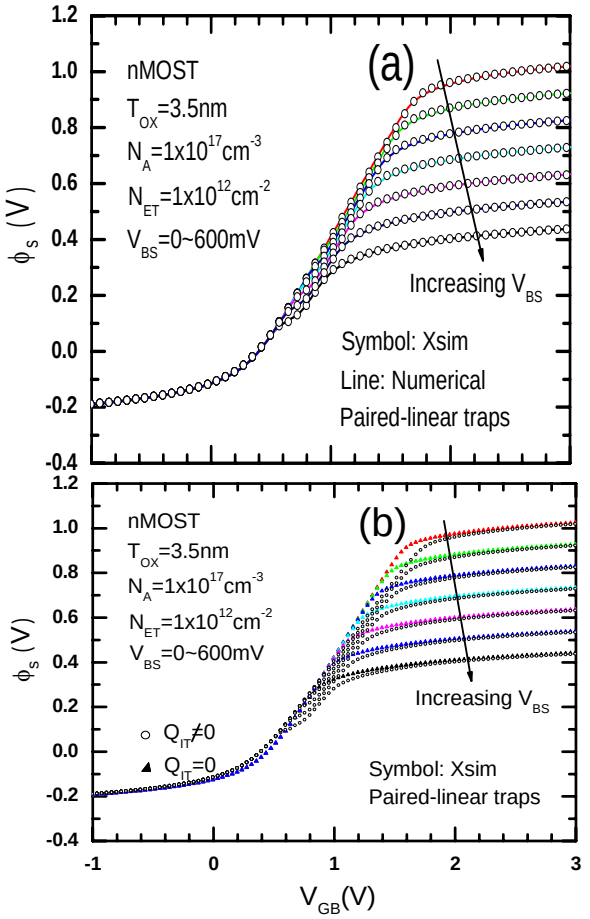

Fig. 2. Interface-trap effect on surface-potential lineshape as a function of the forward bias applied to the base and source terminals: (a) comparison between the URSP approach and the exact iterative solution, and (b) comparison for devices with and without interface traps. V_{BS} = 0, 100, 200, 300, 400, 500, and 600 mV.

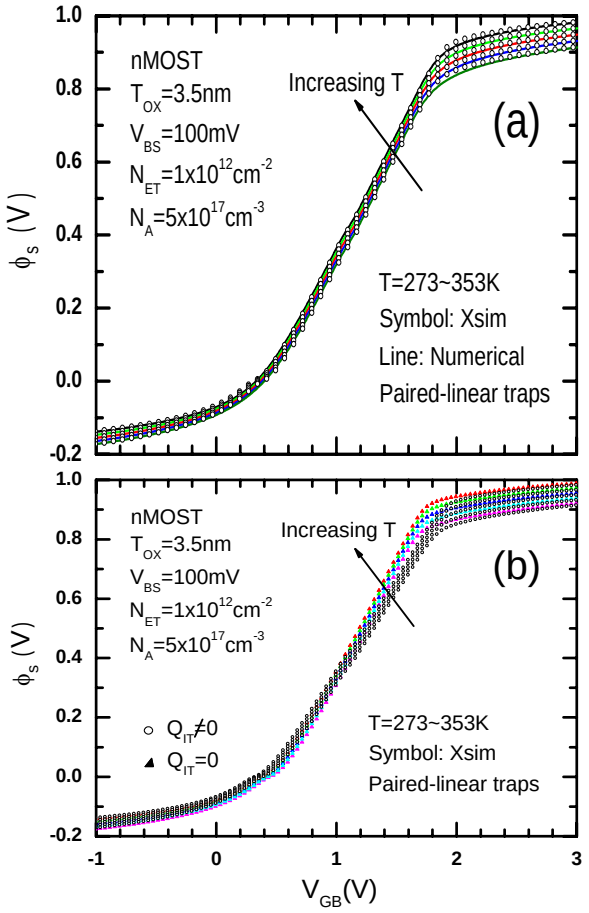

Fig. 3. Interface-trap effect on surface-potential lineshape as a function of transistor temperature: (a) comparison between the URSP approach and the exact iterative solution, and (b) comparison for devices with and without interface traps. T = 273, 293, 313, 333, and 353 K.

$E = E/E_G$ is normalized to the silicon energy gap E_G. D_{ET0} is determined by the given total electron-trap density N_{ET} in (10a), whereas D_{HT0} is solved by (9), and the total hole-trap density N_{HT} can be computed from (10b).

The surface potential ϕ_s without interface traps can be solved as the initial ϕ_s based on (1) to (5), then the total interface-trap charge Q_{IT} can be computed from (6)-(10). In order to obtain the final surface potential for devices with interface traps, the surface potential is computed by several iterations. For each iteration, the surface potential is computed using the URSP approach by replacing Φ_{MS} with $\Phi_{MS} - Q_{IT}/C_{ox}$. After several iterations, the final URSP solutions with interface traps can be obtained and benchmarked with the exact iterative ϕ_s solutions rigorously solved from (1) and (2).

3. RESULTS AND DISCUSSIONS

Figure 1 shows the dependence of the surface potential and gate capacitance on the interface-trap density. The ϕ_s and C_{gg} curves are distorted increasingly as the neutral electron-trap density is increased as shown in Figs. 1(a) and 1(b). The dependence of ϕ_s and C_{gg} on interface-trap density indicates that the extraction of device parameters from experimental measurements should consider interface-trap effect, especially for midlife transistors with high interface-trap concentrations. The lineshape is drastically impacted when the interface-trap density is above 1.0×10^{12} cm^{-2}. When the trap density is lower than 1.0×10^{10} cm^{-2}, the interface-trap effect on surface potential is very small since Q_{IT}/C_{ox} is smaller than 1.62 mV even if all the traps capture electrons or holes for devices with T_{ox} = 3.5 nm. For a given transistor, the C–V lineshape distortion enables us to extract the interface-trap density from experimental data by tuning the trap density as shown in Fig. 1(c).

The effect of interface traps on the surface potential as a function of the forward bias or the injected minority carrier concentration is shown in Fig. 2. The surface potential can be shifted up to 0.1 V by interface-trap charges in the sub-threshold region as shown in Fig. 2(b). The interface-trap density is $N_{ET} = 1.0\times10^{12}$ cm^{-2}, which can be generated during repeated program-erase cycling in nonvolatile floating-gate and SONOS memory transistors [8]. At increasing forward bias, the surface potential is increasingly distorted because the interface-trap charge Q_{IT} is a function of surface carrier concentration, which is exponentially

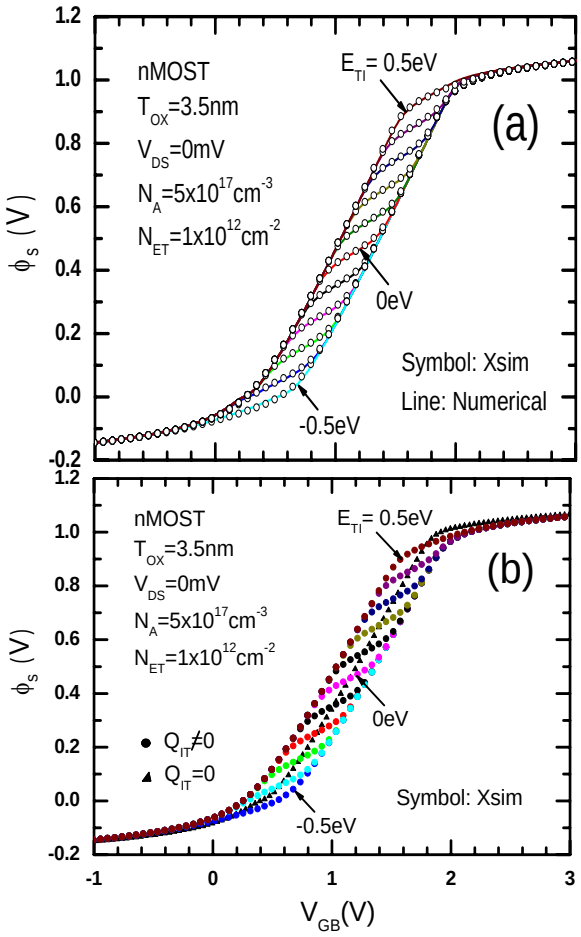

Fig. 4. Effect of discrete energy-level position of interface traps in silicon energy gap on the surface-potential lineshape with E_{TI} = –0.5 to +0.5 eV in 0.1-eV steps: (a) comparison between the URSP approach and the exact iterative solution, and (b) comparison for devices with and without interface traps.

proportional to the forward bias. The phenomenon indicates that high concentration of interface traps can be identified at large forward bias.

Fig. 3 shows the temperature dependence of interface traps on the surface potential. The temperature is varied from 273 to 353 K with 20-K steps. The temperature dependence of surface-potential characteristics is mainly determined by the exponential dependence of the intrinsic carrier concentration $n_i \propto \exp(-E_G/2kT)$, which is also a function of temperature. The surface-potential changes show that temperature fluctuation (e.g., $\Delta T \sim 5$ K) during experimental measurements gives negligible influence on device characteristics.

Fig. 4 shows the surface-potential distortions from interface traps at different energy levels, covering from the slowest and deepest traps around the silicon mid-gap ($E_{TI} = E_T - E_I = 0$) to the fastest and shallowest traps near the conduction- and valence-band edges ($E_{TI} \pm 0.5$ eV). The surface-potential curve (triangle line) without interface traps varies smoothly while the discrete traps significantly distort the surface-potential lineshapes, as shown in Fig. 4(b). The curve distortion would increase at a large interface-trap density. The significant lineshape distortions suggest that the discrete energy level of interface traps can be easily extracted from midlife transistors with high concentration of interface traps than in unstressed devices with low concentration of interface traps.

4. CONCLUSION

In conclusion, the interface-trap density at the SiO_2/Si interface can significantly impact device characteristics such as the gate capacitance and surface potential, which is a key parameter to model the drain-source current. The interface-trap effect due to the trapped charge is small for unstressed or low stressed devices, but it becomes prominent as the increase of transistor operation or stress time, especially important for a midlife device with high interface-trap density. The explicit analytic URSP approach offers a simple way with computational efficiency and device physics to track the generation of interface traps and their properties along the surface channel region.

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