A Unified Compact model for FinFET and Silicon Nanowire MOSFETs

Guojun Zhu, Xing Zhou, Guan Huei See, Shihuan Lin, Chengqing Wei, and Junbin Zhang

School of Electrical & Electronic Engineering, Nanyang Technological University
Nanyang Avenue, Singapore 639798, exzhou@ntu.edu.sg

ABSTRACT

A unified compact model for FinFET and silicon-nanowire MOSFETs including all major short-channel effects is presented. The source–drain symmetry, which is a fundamental feature of an ideal MOSFET, is preserved. The unified compact model is validated with experimental data including higher-order derivatives of the drain current for non-classical MOSFETs.

Keywords: Unified compact model, FinFET, silicon nanowire, Gummel symmetry.

1 INTRODUCTION

As conventional bulk MOSFETs are reaching their scaling limits, Gate-All-Around (GAA) silicon-nanowire (SiNW) [1] and double-gate (DG) [2] MOSFETs are viewed as promising candidates for future CMOS technology due to their superb control of short-channel effects. In this paper, we present a unified compact model for both FinFETs and SiNW MOSFETs. All major short-channel effects are built into the core model without violating source–drain symmetry. The unified compact model is verified with experimental data including the higher-order derivatives of the drain current for non-classical MOSFETs. The model has been implemented in Verilog-A for circuit simulation.

2 MODEL FORMULATIONS

2.1 Current Model for Symmetric-DG MOSFETs

Following [3], the expression for I_{ds} is given as:

$$I_{ds} = 2\mu_{eff\,0} C_{ox} \frac{W}{L}\left(V_{gf} - \overline{\phi_s} + 2v_{th}\right)V_{ds,eff} \qquad (1)$$

where $\mu_{eff\,0}$ is the lateral and vertical field-dependent mobility, C_{ox} is the gate oxide capacitance, and L and W are the gate length and width. Surface potential can be explicitly expressed as:

$$\phi_s\left[V_c(y)\right] = V_{gf} - 2v_{th}\mathcal{L}\left\{\frac{\Upsilon_i}{2\sqrt{v_{th}}} e^{(V_{gf}-V_c)/2v_{th}}\right\} \qquad (2)$$

where $\mathcal{L}\{w\}$ is the *Lambert W* function and $\Upsilon_i = (2q\varepsilon_{Si}n_i)^{1/2}/C_{ox}$. Zero-field potential can be expressed explicitly in terms of the surface potential [4].

Inversion charge is expressed in terms of both surface and zero-field potentials:

$$V_{gt,c}(V_c) = \Upsilon_i\sqrt{v_{th}e^{\frac{\phi_s(V_c)-V_c}{v_{th}}}}\,\sin\left(\frac{\Upsilon_i C_{ox}}{\varepsilon_{Si}}\frac{T_{Si}}{4v_{th}}\sqrt{v_{th}e^{\frac{\phi_0(V_c)-V_c}{v_{th}}}}\right). \qquad (3)$$

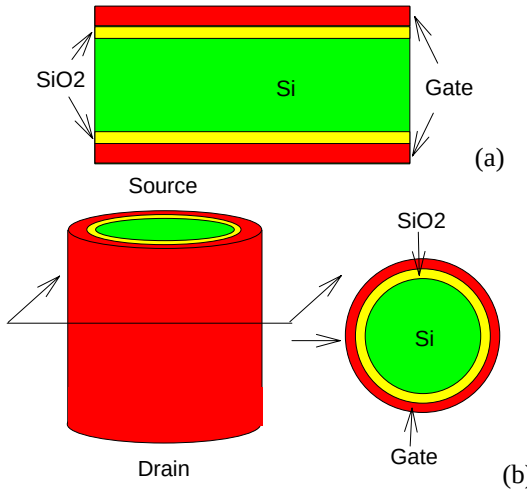

Fig 1. Schematic of an ideal (a) symmetric-DG MOSFET and (b) GAA SiNW MOSFET.

2.2 Current Model for SiNW MOSFETs

A surface potential based current model is formulated similar to that of symmetric-DG (s-DG) MOSFETs.

After integrating Poisson's equation and applying boundary conditions, the following coupled equation can be obtained:

$$V_{gf} - \phi_s = \Upsilon_i\sqrt{v_{th}}e^{(\phi_s-V_c)/2v_{th}}\sqrt{1-e^{-(\phi_s-\phi_0)/2v_{th}}}\,. \qquad (4)$$

In strong inversion, $e^{-(\phi_s-\phi_0)/2v_{th}} << 1$, by simple inspection it can be neglected in (4). The remaining equation can be solved, which results in the single-piece surface potential expression using the *Lambert W* function:

$$\phi_s\left[V_c(y)\right] = V_{gf} - 2v_{th}\mathcal{L}\left\{\frac{\Upsilon_i}{2\sqrt{v_{th}}} e^{(V_{gf}-V_c)/2v_{th}}\right\}. \qquad (5)$$

It can be observed that the above surface potential solution is the same with that for the sDG MOSFET except for the gate oxide capacitance $C_{ox} = \varepsilon_{ox}/[R\ln(1 + T_{ox}/R)]$ due to the difference in the coordinate system.

The zero-field potential for SiNW can be explicitly expressed in terms of the surface potential:

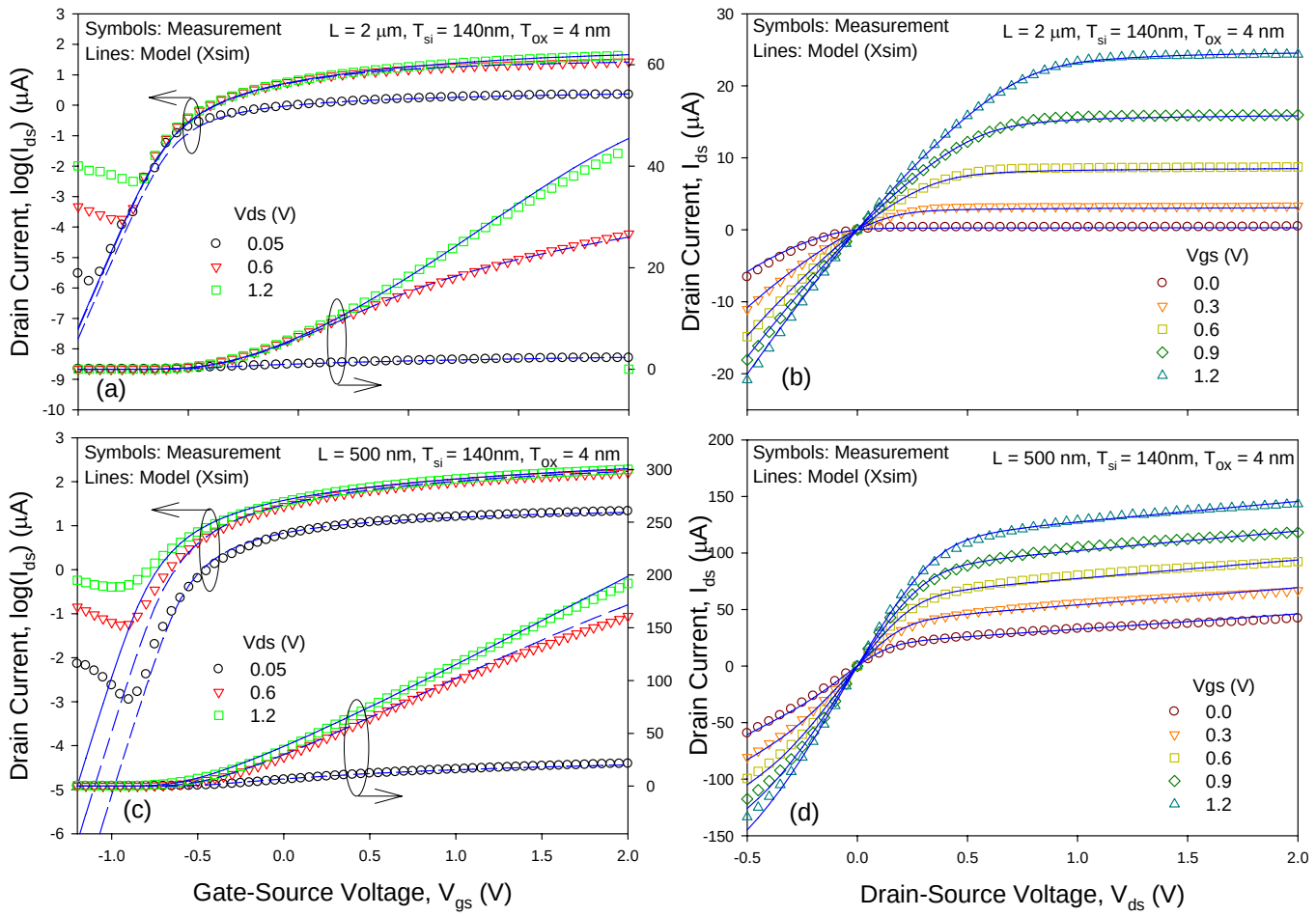

Fig. 2. Drain current characteristics in comparison with measurement data for (a) long channel I_d–V_g, (b) long channel I_d–V_d, (c) short channel I_d–V_g, and (d) short channel I_d–V_d.

$$\phi_0\left[V_c(y)\right]=\phi_s\left[V_c(y)\right]+2v_{th}\ln\left\{\frac{-1+\sqrt{1+4\omega}}{2\omega}\right\} \tag{6}$$

where

$$\omega=\delta e^{\frac{\phi_s\left[V_c(y)\right]-V_c(y)}{v_{th}}} \tag{6a}$$

$$\delta=\frac{R^2}{8\varepsilon_{si}L_i^{\,2}} \tag{6b}$$

$$L_i=\sqrt{v_{th}\varepsilon_{si}/qn_i}\,. \tag{6c}$$

Equation (4) can be further transformed into:

$$V_{gf}-\phi_s=\frac{R\varepsilon_{si}v_{th}}{2L_i^{\,2}C_{ox}}e^{(\phi_s+\phi_0-2V_c)/2v_{th}}\,. \tag{7}$$

The right-hand side of (7) is taken as the expression for the inversion charge:

$$V_{gt,c}\left(V_c\right)=\frac{R\varepsilon_{si}v_{th}}{2L_i^{\,2}C_{ox}}e^{(\phi_s+\phi_0-2V_c)/2v_{th}}\,. \tag{8}$$

The final expression for I_{ds} is given as:

$$I_{ds}=2\mu_{eff\,0}C_{ox}\frac{\pi R}{L}\left(V_{gf}-\overline{\phi_s}+2v_{th}\right)V_{ds,eff} \tag{9}$$

which is consistent with that of sDG MOSFETs.

Second-order effects such as drain-induced barrier lowering (DIBL), channel-length modulation (CLM), series resistance, field-dependent mobility, quantum mechanical effect, poly-depletion effect, etc., are built into the core model following the steps given in [6-8]. Special efforts have been made to ensure the Gummel symmetry condition is not violated after including all the second-order effects.

3 RESULTS AND DISCUSSION

The unified compact model is verified with both long- and short-channel FinFET data. Fig. 2 shows that the model gives very good agreement with the recent measurement data.

Fig. 3 shows the measured and modeled high-order derivative of the Gummel symmetry test (GST) for the short-channel FinFET. The model reproduces all the high-order derivatives accurately with all major short-channel effects included. It is believed to be the first demonstration of measured higher-order derivatives of the GST for non-classical MOSFETs.

NSTI-Nanotech 2009, www.nsti.org, ISBN 978-1-4398-1784-1 Vol. 3, 2009

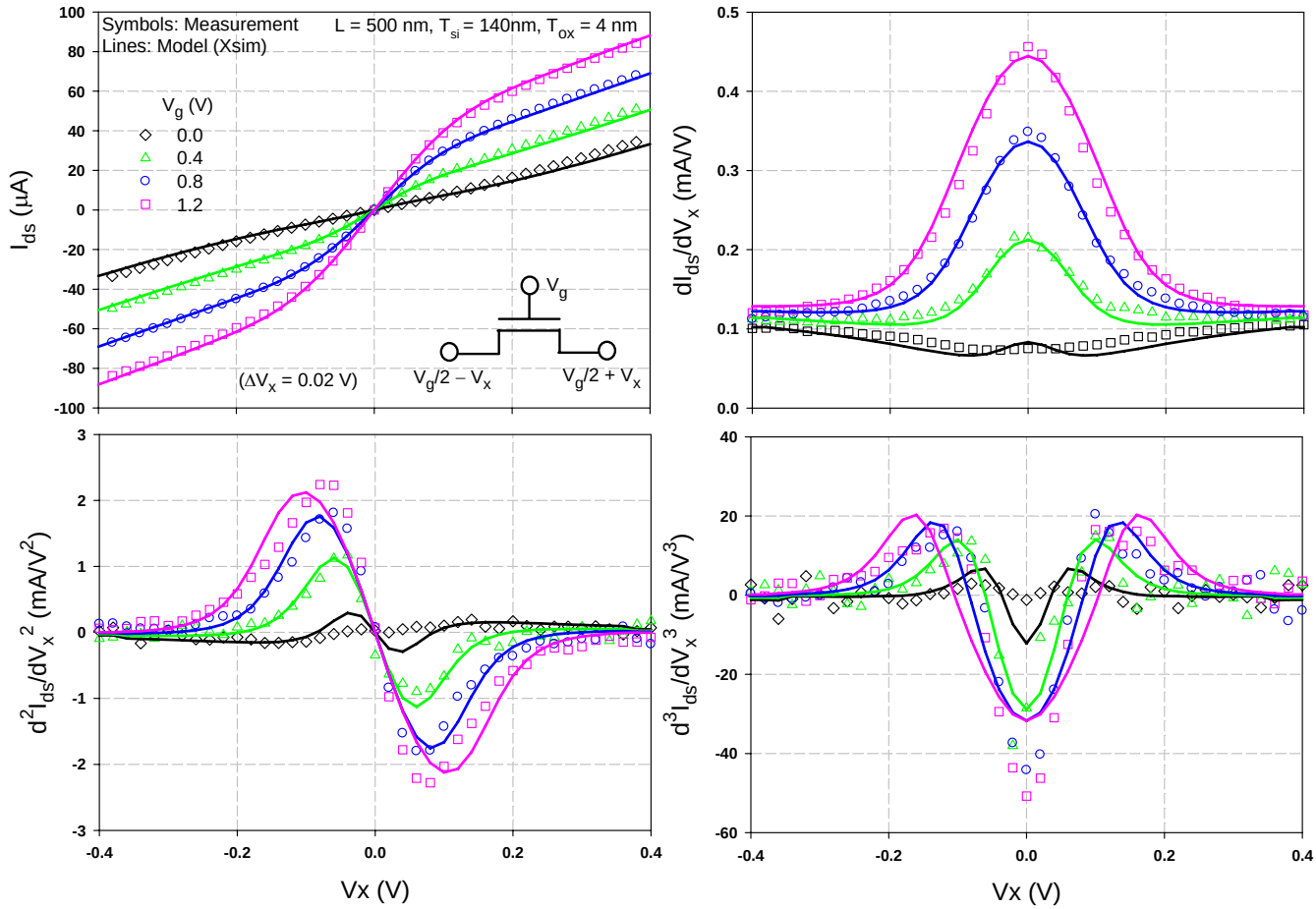

Fig. 3. GST comparison of .the lines complete model (a) drain current and its (b) first, (c) second, and (d) third-order derivatives with experimental data. GST test circuit is given in the inset of (a).

Fig. 4 shows the calibrated model playback in comparison with Medici numerical simulation. Due to very few model parameters, the parameter extraction procedure is straightforward and no binning is required. The model demonstrates very good geometry scaling capability. As shown in Fig. 4(b), threshold voltage roll-off and subthreshold slope degradation is captured automatically as the gate length reduces. The model also shows good scalability over nanowire radius as demonstrated in Fig. 4(c).

The unified model is also verified with the recently fabricated ultra-narrow SiNW MOSFETs [1] and excellent agreement has been achieved including all high-order derivatives of the drain current. The results are not shown in this paper. The model has been coded in Verilog-A. Fig. 5 shows the circuit simulation results which are obtained from Hspice simulation, in which the model parameters are extracted from the fabricated real device [1]. Fig. 5(a) demonstrates the DC transfer characteristics of an inverter at different V_{dd}. Fig. 5(b) shows the transient characteristics of a 21-stage ring oscillator.

4 CONCLUSION

In conclusion, a unified compact model for SiNW and FinFET is presented. The model shows excellent agreement with experimental data including all the high-order derivatives of the drain current. The unified model has also been implemented in commercial simulator using Verilog A language. Stable and consistent circuit simulation has been achieved and demonstrated.

Acknowledgment: This work was supported in part by Nanyang Technological University under Grant RGM30/03 and in part by Semiconductor Research Corporation under Grant 2004-VJ-1166G. G. J. Zhu would like to thank Mr. Sun Yongshun for providing the silicon nanowire devices for model verification and for the help in setting up the measurement.

REFERENCES

[1] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi, A. O. Adeyeye, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Ultra-narrow silicon nanowire gate-all-around

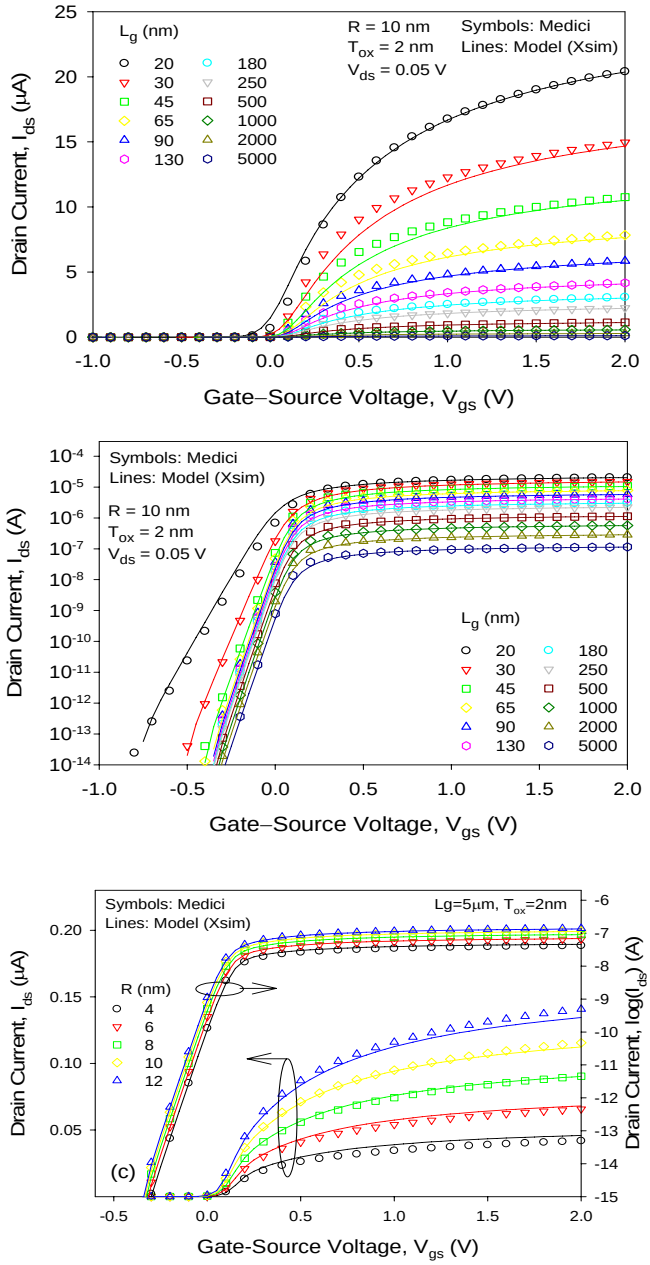

Fig. 4. Model comparison with Medici numerical simulation (a) at different channel lengths in linear scale, (b) at different channel lengths in log scale. Threshold voltage roll-off and subthreshold slope degradation are automatically captured without binning (c) at different nanowire radius.

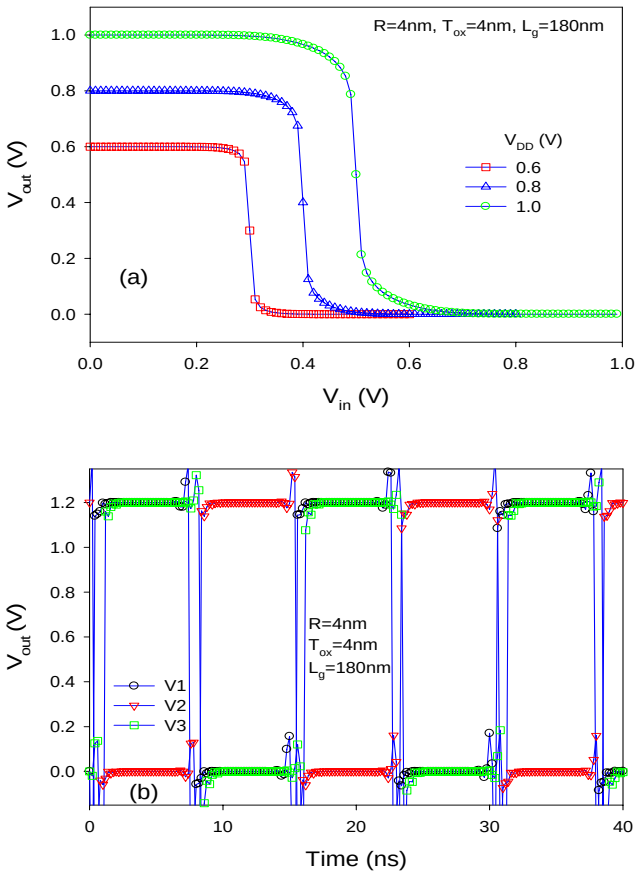

Fig. 5. Hspice simulation of (a) the DC transfer characteristics of an inverter and (b) the transient characteristics of a 21-stage ring oscillator.

CMOS devices: impact of diameter, channel-orientation and low temperature on device performance," in *IEDM Tech. Dig.*, 2006, pp. 547–550.

[2] F. Balestra, S. Cristoloveanu, M. Benachirm, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance," *IEEE Electron Device Lett.*, vol. EDL-8, no.9, pp. 410–412, Sep. 1987.

[3] G. J. Zhu, G. H. See, S. H. Lin, and X. Zhou, "'Ground-Referenced' Model for Three-Terminal Symmetric Double-Gate MOSFETs with Source–Drain Symmetry," *IEEE Trans. Electron Devices*, Vol. 55, No. 9, pp. 2526–2530, Sep. 2008.

[4] W. Z. Shangguan, X. Zhou, K. Chandrasekaran, Z. M. Zhu, S. C. Rustagi, S. B. Chiah, and G. H. See, "Surface-potential solution for generic undoped MOSFETs with two gates," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 169–172, Jan. 2007.

[5] W. Bian, J. He, Y. Tao, M. Fang, and J. Feng, "An Analytic Potential-Based Model for Undoped Nanoscale Surrounding-Gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2293–2303, Sep. 2007.

[6] G. H. See, X. Zhou, K. Chandrasekaran, S. B. Chiah, Z. M. Zhu, C. Q. Wei, S. H. Lin, G. J. Zhu, and G. H. Lim, "A compact model satisfying Gummel symmetry in higher order derivatives and applicable to asymmetric MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 624–631, Feb. 2008.

[7] S. B. Chiah, X. Zhou, K. Chandrasekaran, W. Z. Shangguan, G. H. See, and S. M. Pandey, "Single-piece polycrystalline silicon accumulation/depletion/inversion model with implicit/explicit surface-potential solutions," *Appl. Phys. Lett.*, Vol. 86, No. 20, 202111, May 2005.

[8] G. H. See, X. Zhou, G. Zhu, Z. Zhu, S. Lin, C. Wei, J. Zhang, and A. Srinivas, "Unified regional surface potential for modeling common-gate symmetric/asymmetric double-gate MOSFETs with quantum-mechanical effects," in *Proc. NSTI Nanotech*, Boston, Jun. 2008, pp. 756–759.