Compact Modeling of Dynamic Threshold Voltage of Nanoscale FinFET High K Gate Stack and Application in Circuit Simulation

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Abstract **- A modeling study of dynamic threshold voltage in high K gate stack is reported in this paper. Both slow transient (STCE) and fast transient charging effect (FTCE) are included in this model. Finally, this model is applied in FinFET reliability and circuit performances are simulated. The result shows that, the drain circuit (I_d) degradation in FinFET is much more obvious than normal MOSFETs with the same processes and the variation of I_d is slower in higher temperature. However, the dynamic threshold voltage in high K stack seems not affect the delay time of reverser simulated by HSPICE.**

1 Introduction

The aggressive scaling down of MOSFETs has driven the physical thickness of SiO_2 gate dielectrics to its limit [1]. To release the unendurable gate leakage due to ultra thin gate oxide, high K dielectrics such as HfO_2 became a promising candidate for future nano-scaled devices [2-7]. However, the threshold voltage instability induced by traps is one of the challenges for the use of high K dielectrics in future MOS technologies [8, 9]. In order to predict and optimize the performance of nano-scaled integrate circuit, a model including both slow (STCE) and fast transient charging effect (FTCE) [10] is presented. Furthermore, this model is applied in predicting the performance of FinFET with high K gate stack.

2 Principle of Dynamic Threshold Voltage in High K Gate Stack

Due to the high density of structure defects, high K gate dielectric is easy to trap carriers tunneling from channel. A typical schematic view of charge trapping in high K dielectric is shown in Fig.1. Electrons in channel transfer to the high K layer by direct tunneling under positive gate voltage. Charges trapped at the interface of high K and oxide induced fast transient charging effect (FTCE) [10] and some travel further into the high K layer reflect a slow transient charging effect (STCE). Charge accumulated in the high K layer causes threshold voltage variation (ΔV_{th}) and drain current degradation [10].

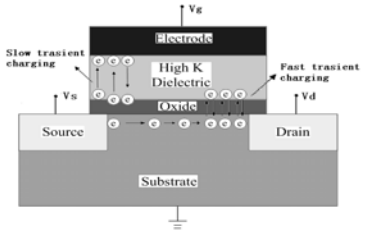

Fig.1 Schematic view of charge trapping in high K dielectric layer. The distance of charges transferred in high K layer represents fast and slow transient charging.

3 Model Development

This model supposed that:

(1) The threshold voltage shift (ΔV_{th}) is a function of stress time (t) and injected charge density;

(2) ΔV_{th} is mainly induced by the traps in the high K layer, and the increase of new defects can be neglected.

The distinguish between high K model and SiO_2 model is that, the distribution of capture cross section (σ) in SiO_2 is uniform [11][12] while in high K layer is a function of stress voltage V_s, as shown in Fig.2. [13].

$$\sigma = \sigma_0 V_s^{\,b} \tag{1}$$

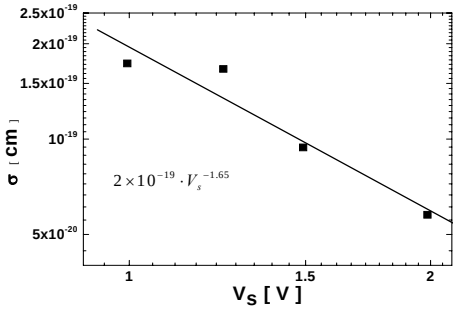

Fig.2 Dependence of the capture cross section (σ) as a function of stress voltage V_s for HfO_2 gate dielectrics.

The trapped charge density n_t is written as a function of the total interface trap density N_{it0} and injected charge density N_{inj0} [13].

$$n_t = N_{it0}[1-\exp(-N_{inj0}\cdot\sigma)^{\beta}] \tag{2}$$

Where β is a constant and σ is the capture cross section.

Combining Eqs.2 and 3, the threshold voltage shift (ΔV_{th}) is expressed as a function of the maximum threshold voltage shift (ΔV_{thmax}) and trapped charge density (n_t). [13].

$$\Delta V_{th} = \Delta V_{th\max}[1 - C\exp(-N_{inj0}t^a\sigma)] \qquad (3)$$

Where $N_{inj0} = J_{g0}/q$, $\sigma = \sigma_0 V_s^b$, J_{g0} is the gate leakage current density, C is a fitting parameter close to one. ΔV_{thmax} is supposed to be the maximum threshold voltage variation. Following the principle in *Section II*, ΔV_{thmax} is resulted from carriers trapped both at the interface and in the high K layer. In our model, traps at the interface of high K layer and oxide are considered as steps. Only carriers on these steps are able to transfer further into the high K layer and induce the maximum threshold voltage variation (ΔV_{thmax}). Therefore, ΔV_{thmax} is determined by not only the total density of interface states (N_{it0}), but also the stress voltage V_s. Consequently, ΔV_{thmax} is written as the function of the temperature T and stress voltage V_s.

$$\Delta V_{th\max} = \Delta V_{th0} \cdot AT\exp(BV_s) \qquad (4)$$

$$\Delta V_{th0} = \frac{qN_{it0}}{C_{gate}} = \frac{qN_{it0}}{\varepsilon_0\varepsilon_{HfO_2}/t_{HfO_2}} \qquad (5)$$

Combining Eqs.1-5, the final expression of dynamic threshold voltage ΔV_{th} is

$$\Delta V_{th} = AT \cdot \frac{qN_{it0}}{\varepsilon_0\varepsilon_{HfO_2}/t_{HfO_2}} \cdot \exp(BV_s)[1 - C\exp(-N_{inj0}t^a\sigma_0 V_s^b)] \qquad (6)$$

Meanings of parameters in Eq. 6 are shown as follows respectively:
A, B, C and b are fitting parameters.
a is the degradation exponent.
V_s is the stress gate voltage.
k is the Boltzmann constant.
T is the process temperature.
N_{it0} is the initial trapped density in HfO_2.
t_{HfO2} is the thickness of the HfO_2 file.
N_{inj0} is the carrier density injected into the gate dielectric, which can be calculated from the gate leakage current density J_{g0}.
t is the stress time.
σ_0 is the capture section.

When stress time t tends to infinite, ΔV_{th} becomes a constant, which reflects the slow transient charging effect (STCE) induced by the carriers trapped in the deep position of high K layer; while, at the beginning several microseconds of measurement, ΔV_{th} is a function of stress time, which defined as fast transient charging effect (FTCE) caused by carriers transferred at the interface of high K layer and oxide. .

4 Experiment and Discussion

In order to test our analytic model, the high K gate stack structure is measured and then ΔV_{th} versus transient time t is extracted. Eq. 6 is used to fit the experimental data to extract *a, b, A, B* and *C*.

For the experimental sample HfO_2 gate stack with 4.5nm thickness and 800℃ annealing under the N_2 atmosphere, the measured stress condition is from 1.6V to 2V with the transient time 1 second [14]. The threshold voltage instability is plotted in Fig.3 (a) in points and the model prediction is also shown in this figure in lines. It is easily found that the analytic model matches well with the experimentally measured ΔV_{th}.

Under the stress condition of 1.8V and 2V with the transient time 1 second, the experimental sample 3nm HfO_2 gate stack with 600℃, N_2 annealing shows the significant difference compared with the first sample in the dynamic behavior of the threshold voltage as shown by the points in Fig.3 (b). Here, the induced trap density demonstrates evident saturation trend at the early transient time. One can observe that, however, the analytic model matches well with the experimentally measured V_{th} shifts as shown in Fig. 3(b). The results show that higher V_g causes larger V_{th} variation.

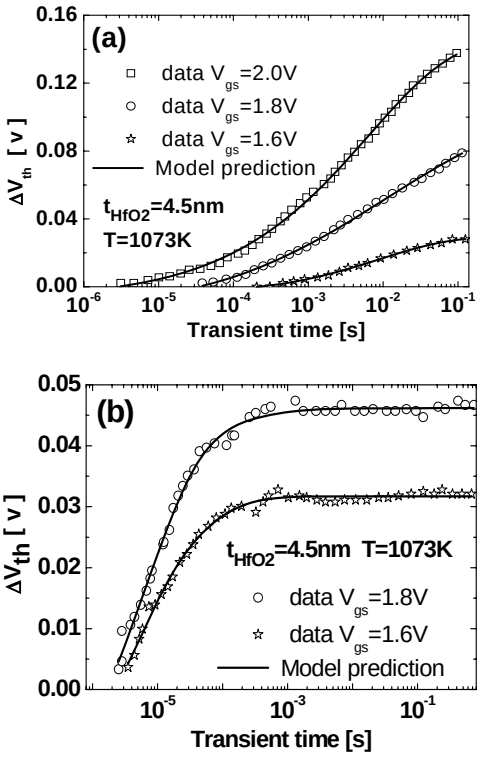

Fig.3 The comparison of analytic model prediction and the experiment-extracted data in showing the threshold voltage increase due to trapping mechanism. (a) 4.5nm HfO_2, 800℃, N_2 annealing. (b) 3nm HfO_2, 600℃, N_2 annealing. Higher V_g causes larger V_{th} variation.

The detail of calculation and parameters are shown as follows: At process temperature $T_1 = 800C^\circ = 1073K$, the threshold voltage shift ΔV_{th} is shown in Eqs. 7 and 8, and corresponding parameters are listed in Table Ⅰ.

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$$\Delta V_{th(1073K)} = \frac{A_{(1073K)} T_{(1073K)} q N_{it0}}{\varepsilon_0 \varepsilon_{HfO_2} / t_{HfO_2(1073K)}} \cdot \exp(B_{(1073K)} V_s) \quad (7)$$
$$\cdot[1 - C_{(1073K)} \exp(-N_{inj0} t^{a_{(1073K)}} \sigma_{0(1073K)} V_s^{\ b})]$$

$$A_{(1073K)} T_{(1073K)} \cdot \frac{q N_{it0}}{\varepsilon_0 \varepsilon_{HfO_2} / t_{HfO_2(1073K)}} = 5.5 \times 10^{-5} \quad (8)$$

TABLE Ⅰ
SPECIFIC PARAMETERS IN THE CONDITION OF 4.5NM HFO_2, 800℃, N_2 ANNEALING.

$T_1 = 1073K$	$t_{HfO_2(1073K)} = 4.5nm$	$N_{it0} = 5 \times 10^{10} cm^{-2}$
$\varepsilon_{HfO_2} = 5$	$N_{inj0} = 10^{18} cm^{-2}$	$A_{(1073K)} = 9.6 \times 10^{-8}$
$B_{(1073K)} = 4$	$a_{(1073K)} = 0.365$	$b = 1.65$
$\sigma_{0(1073K)} = (1.92 \sim 2) \times 10^{-18} cm^2$		$C_{(1073K)} = 1.1$

When T_1= 800℃ transfers to T_2= 600℃, meanwhile the thickness of HfO_2 varies from *4.5nm* to *3nm*, Equation (6) is also adapted, except changing temperature T and high K layer thickness t_{HfO2}.

Although ΔV_{thmax} includes fitting parameter and dependents on the process situation such as temperature, the following equations provide experience calculation for ΔV_{thmax} under different process temperature.

Similar to Eq.7, $\Delta V_{th(873K)}$ is written as

$$\Delta V_{th(873K)} = A_{(873K)} T_{(873K)} \cdot \frac{q N_{it0}}{\varepsilon_0 \varepsilon_{HfO_2} / t_{HfO_2(873K)}} \quad (8)$$
$$\cdot \exp(B_{(873K)} V_s)[1 - C_{(873K)} \exp(-N_{inj0} t^{a_{(873K)}} \sigma_{0(873K)} V_s^{\ b})]$$

$$A_{(873K)} = A_{(1073K)} \cdot \exp(\frac{T_1}{T_2}) = A_{(1073K)} \cdot \exp(\frac{1073}{873}) \quad (9)$$

$$B_{(873K)} = \frac{T_2}{T_1} B_{(1073K)} = \frac{873}{1073} B_{(1073K)} \quad (10)$$

$$C_{(873K)} = C_{(1073K)} \times \frac{T_1}{T_2} = 1.1 \times \frac{1073}{873} = 1.35 \quad (11)$$

The final expression of ΔV_{th} in case of 3nm HfO_2, 600℃, N_2 annealing is

$$\Delta V_{th(873K)} = A_{(1073K)} \cdot \exp(\frac{1073}{873}) \cdot \frac{1073}{873} \cdot \frac{q N_{it0}}{\varepsilon_0 \varepsilon_{HfO_2} / t_{HfO_2(873K)}}$$
$$\cdot \exp(\frac{1073}{873} B_{(1073K)} V_s)[1 - C_{(873K)} \exp(-N_{inj0} t^{a_{(873K)}} \sigma_{0(873K)} V_s^{\ b})] \quad (12)$$
$$= \frac{5.5 \times 10^{-5} \times \exp(\frac{1073}{873}) \times (\frac{3}{4.5})}{0.8} \cdot \exp(0.8 B_{(1073K)} V_s)$$
$$\cdot [1 - C_{(873K)} \exp(-N_{inj0} t^{a_{(873K)}} \sigma_{0(873K)} V_s^{\ b})]$$
$$= 14.5 \times 10^{-5} \exp(0.8 B_{(1073K)} V_s)$$
$$\cdot [1 - C_{(873K)} \exp(-N_{inj0} t^{a_{(873K)}} \sigma_{0(873K)} V_s^{\ b})]$$

The drain current (I_d) versus trapping time (t) under various stress voltage (V_g) with different process temperature and high K dielectrics thickness is shown in Fig.4. In Fig.4 (a), I_d increases as stress voltage V_g increased; In Fig.4 (b), the variation of I_d to a constant is gentler in high process temperature than in lower one, meanwhile, I_d is larger with thinner high K dielectrics thickness.

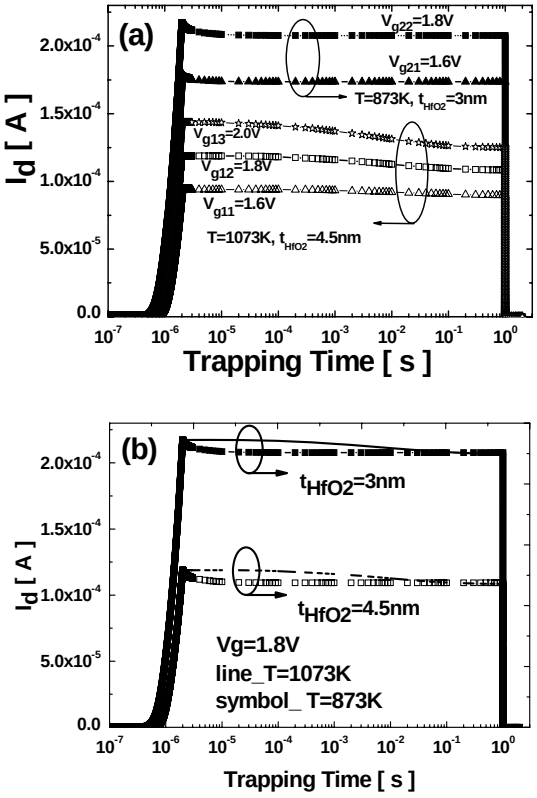

Fig.4 (a) I_d variation during trapping time. (b) I_d varied with T and t_{HfO2} with constant V_g. I_d increased with thinner t_{HfO2} and higher T.

5 Model Application in FinFET Performance Prediction

FinFET is one of the most promising device structures in its perfect immunity to the short channel effect (SCE) [15, 16]. The schematic view of bulk FinFET is shown in Fig.5. L_g is the gate length, H_g is the Fin height and W_{fin} is the width of Fin.

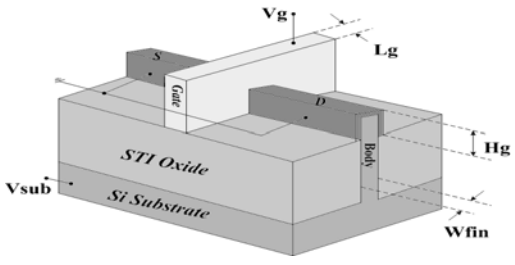

Fig.5 Schematic view of bulk FinFET.

It is seems that, the cooperation of FinFET and high K gate stack is a perfect idea for improving device performance, however, both experiments [10] and simulation show some contrary results. Fig.6 shows the

relationship between drain current (I_d) and trapping time (t) under various stress voltage (V_g) with different high K dielectrics thickness. Except for a larger drain current, FinFET exhibits a more obvious variation of I_d than normal MOSFETs. It is means that, high K gate stack applied in FinFET induced more severe FTCE. Therefore, measure method and corresponding delay time are likely to affect the results of experiments.

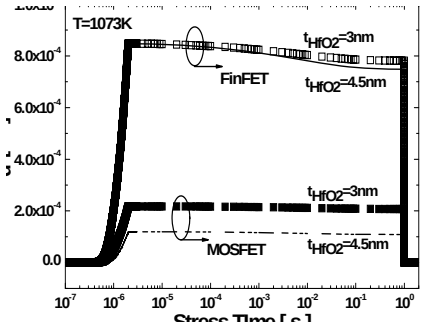

Fig.6 I_d of FinFET and normal MOSFETs varied with $T=800℃$ and t_{HfO2}=4.5nn and 3nm under constant V_g. I_d increased with thinner t_{HfO2}. FinFET exhibits a more obvious variation of I_d and a longer decreasing time.

In order to demonstrate whether high K gate stack will bring delay to circuit, a ring oscillator with 21 stages is designed for testing. The result in Fig.7 shows that, besides some original gate delay, there is not any delay caused by high K dielectrics.

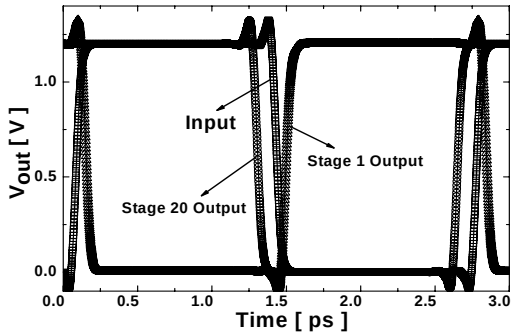

Fig.7 Out put of ring oscillator with 21 stages with (line) and without (symbol) high K dielectrics.

6 CONCLUSION

A model of dynamic threshold voltage in high K gate stack including both slow transient (STCE) and fast transient charging effect (FTCE) is reported in this paper. This model is well matches with experimental data and the variation of drain current with stress time is simulated.

. ACKNOWLEDGEMENTS

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