Design study of CNT transistor layouts for analog circuits

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ABSTRACT

In this work, CNTFET technology is explored for a class-A power amplifier. A device structure is proposed meeting the specifications of the PA, and suggestions are made for optimizing the transistor layout w. r. t. highest possible transit frequencies.

Keywords: CNTFET, power amplifier, device simulation, parasitics, compact model

1 INTRODUCTION

So far, CNTFETs have been considered mostly as a replacement for high performance logic applications. Yet, due to the interesting CNT properties [1] and more relaxed demands on device size, it is worth to examine CNTFET technology for high speed analog applications. The high current carrying capability of CNTs suggests their use for e. g., RF power amplifiers, even if hundreds or thousands of CNTs in parallel are needed to achieve considerable output power. A first design approach is given in section 2. Note, that for the time being, regardless of the technological difficulties, identical CNTs are used. Also, the impact of statistical variations and CNT misalignments are studied elsewhere.

A CNTFET suitable for RF power amplifiers should exhibit in general (*i*) a high transconductance, (*ii*) a high current, (*iii*) monotonous transfer and output characteristics in the electrically important bias range, and (*iv*) a high transit frequency over a wide range of drain currents and voltages. An appropriate device design is given in section 3. Besides the design parameters, material parameters like bandgap and different work functions worsen or improve the aforementioned effects (see e. g. [2] for more details). Due to a relative small bandgap of around $0.6e$V in comparison to SIFETs, band-to-band tunneling can additionally affect the device behavior. For classical analog applications, band-to-band tunneling needs to be suppressed.

For the intrinsic device design optimization we use an efficient and fast numerical device simulator [3], [4] especially developed for, but not restricted to, partially gated CNTFETs. For the time being, band-to-band tunneling is not considered within the simulator.

Obviously, the parasitics in a given transistor layout [5] comprising gate, source and drain fingers and the number of tubes in parallel degrade the fundamental high frequency properties of CNTFETs. Consequently, the question arises, how to design feasible analog CNTFET circuits with still superior behavior in comparison to SIFET circuits. The impact of the layout on the maximum operating frequency of the PA and some optimization criteria are studied in section 4. In contrast to [6], we present a detailed layout study with emphasis on partially gated CNTFETs and propose a transit frequency f_T formulation suitable for technology development and layout optimization based on f_T.

2 POWER AMPLIFIER SPECIFICATIONS

The power amplifier to be designed is supposed to provide $1.5m$W to an output load R_L. For simplicity we chose a class A topology. Typically, RF power amplifiers are biased in the saturation region of the output characteristics. While the maximum efficiency is limited to 50%, highest operation frequency around a third of the maximum transit frequency is achievable at least for conventional SIFET devices.

In class-A operation, the signal is amplified during the full signal period. Without signal clipping and assuming negligible device nonlinearity, only the fundamental signal component exists yielding a maximum RF output power of

$$P_\mathrm{rf,out} = \frac{(V_\mathrm{dc} - V_\mathrm{ds,min})^2}{2R_\mathrm{L}}, \tag{1}$$

where $V_\mathrm{dc} - V_\mathrm{ds,min}$ is the magnitude of the RF drain voltage (cf. Fig. 3). The dissipated large-signal DC power is given by

$$P_\mathrm{dc} = \frac{V_\mathrm{dc}(V_\mathrm{dc} - V_\mathrm{ds,min})}{R_\mathrm{L}}. \tag{2}$$

Note, that due to a non-negligible $V_\mathrm{ds,min}$, the maximum efficiency $\eta = \frac{P_\mathrm{rf,out}}{P_\mathrm{dc}}$ is not reached.

The maximum magnitude of the RF drain voltage shall be 2V while $V_\mathrm{ds,min}$ shall not exceed 1V. So, the DC bias point is set to $V_\mathrm{dc} = 3$V. The efficiency than falls to 33%. To provide a power of $P_\mathrm{rf,out} = 1.5m$W, we

need a DC current $I_{\mathrm{dc}} = \frac{1}{\eta V_{\mathrm{dc}}} P_{\mathrm{rf,out}}$ of $1.5mA$. If each CNTFET channel delivers $I_{\mathrm{dc,ch}} = 15\mu\mathrm{A}$, a number of 100 channels in parallel is needed. Additionally we demand the highest possible transit frequency for the transistor.

3 INTRINSIC DEVICE DESIGN

Fig. 1 shows a sketch of the design structure used for numerical device simulation in this work. It represents a unit cell of the multi-tube transistor shown in Fig. 4.

Since the contact configuration essentially influences the device behavior, the dimensions of a unit cell have to be carefully adjusted to approach the power amplifier specifications.

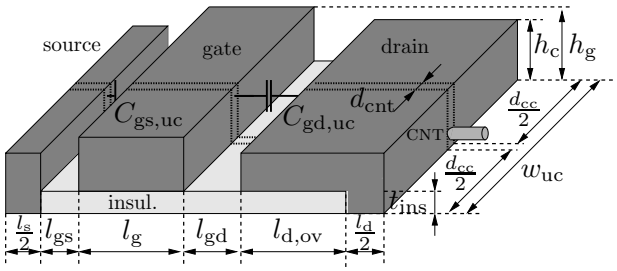

Figure 1: Partially gated CNTFET suitable for analog circuit design. This structure represents a unit cell of a multi-tube and multi-channel transistor.

Due to the drain contact overlap $l_{\mathrm{d,ov}}$ along the gate insulator, source and drain contacts are not symmetrical in contrast to usually fabricated structures. This overlap acts similar to a second gate [7], but simplifies the technology and the circuit design. Hence, ambipolar behavior is suppressed due to the potential barrier under the drain overlap as long as the overlap is long enough. In this example we choose $l_{\mathrm{d,ov}} = 30n\mathrm{m}$. The gate-drain spacer length l_{gd} determines the impact of band-to-band tunneling on the overall device characteristics. To minimize this effect, l_{gd} is set to $20n\mathrm{m}$. The gate length l_{g} equals $50n\mathrm{m}$ to prevent oscillations [8] in the transfer as well as output characteristics. To ensure a high current density, the gate-source spacer length l_{gs} is set to $5n\mathrm{m}$. If this distance is technologically difficult to realize, the spacer can be doped while increasing l_{gs} and ensuring the same high current density. The insulator thickness is $5n\mathrm{m}$. For all simulations we use an undoped CNT with no Schottky barriers for the electrons, a bandgap E_{gap} of $0.6eV$, an effective mass m_{c}^* of $0.05m_0$ and a diameter d_{cnt} of $1.6n\mathrm{m}$.

In contrast to SIFETs, the channel of a multi-tube transistor is discretized. The minimum distance d_{cc} between two neighboring tubes to prevent electrostatic coupling is $2d_{\mathrm{cnt}}$ [9]. Enlarging the tube separation increases the gate width per unit cell $w_{\mathrm{uc}} = d_{\mathrm{cnt}} + d_{\mathrm{cc}}$. The height h_{g} of the metal gate contact is set to $20n\mathrm{m}$ for a fairly high unilateral power gain frequency, whereas the source and drain contact height h_{c} equals $10n\mathrm{m}$. Note, that the value of h_{c} does not significantly affect the parasitic capacitance[1] between the contacts. The contact lengths l_{s} and l_{d} are set to $20n\mathrm{m}$. The minimum parasitic gate capacitance of a unit cell $C_{\mathrm{g,uc}}^{\mathrm{min}} = \bar{C}_{\mathrm{g,uc}} d_{\mathrm{cnt}}$, with $\bar{C}_{\mathrm{g,uc}} = (C_{\mathrm{gd,uc}} + C_{\mathrm{gs,uc}})/w_{\mathrm{uc}}$, is determined by the diameter d_{cnt} of a tube. Note, that $\bar{C}_{\mathrm{g,uc}}$ depends significantly on the spacer lengths. Since these lengths are enforced by device specifications like the suppression of ambipolar behavior, $\bar{C}_{\mathrm{g,uc}}$ is mostly determined by these specifications. For the spacer lengths given in Fig. 1, $\bar{C}_{\mathrm{g,uc}}$ equals $0.04a\mathrm{F}/n\mathrm{m}$.

Fig. 2 and Fig. 3 show the intrinsic transit frequency $f_{\mathrm{T,int}}$ and the output characteristic of the intrinsic device. Note, that peak $f_{\mathrm{T,int}}$ is about $8T\mathrm{Hz}$ for $V_{\mathrm{ds}} = 3\mathrm{V}$.

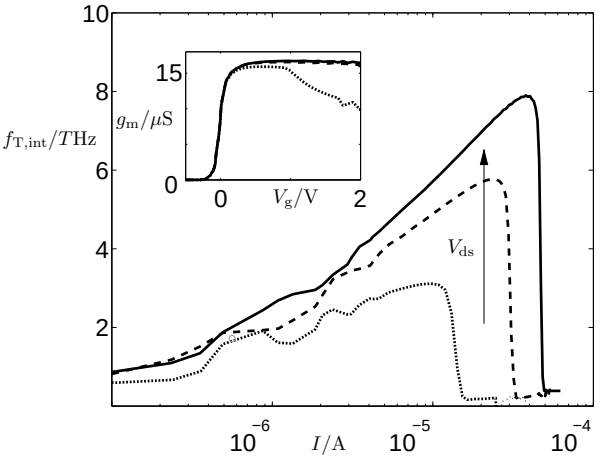

Figure 2: Intrinsic transit frequency $f_{\mathrm{T,int}}$ for $V_{\mathrm{ds}} = \{1\mathrm{V}, 2\mathrm{V}, 3\mathrm{V}\}$. The inset shows the transconductance of the device.

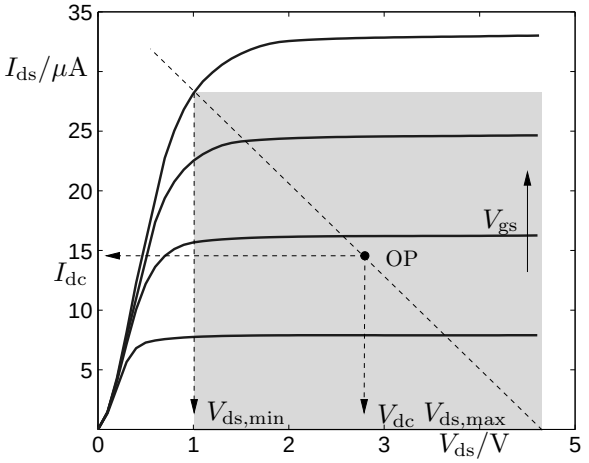

Figure 3: Output characteristic for a single tube for $V_{\mathrm{gs}} = \{0.5\mathrm{V}, \ldots, 2\mathrm{V}\}$. The shaded region is used for power amplification.

[1] All inter-contact capacitances mentioned in this work are calculated by solving the Laplace equation.

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4 LAYOUT OPTIMIZATION

Fig. 4 shows a typical CNTFET layout for PA applications. The maximum output power is increased with multiple CNTs in parallel while the multi-finger structure increases the number of channels per tube. In contrast to SIFETs layout parasitics can dominate the device behavior due to the small intrinsic capacitances $C_{\mathrm{g,int}}$, and, hence, must be taken into account during circuit design.

For further discussions, the layout-induced parasitics are grouped into (*i*) channel parasitics $C_{\mathrm{g,par}}$ and (*ii*) external parasitics $C_{\mathrm{g,ext}}$ mostly dominated by the feed lines (cf. Fig. 4).

The impact of the layout on the device behavior is studied by means of changes in the transit frequency

$$f_{\mathrm{T}} = \frac{1}{2\pi}\frac{g_{\mathrm{m}}}{C_{\mathrm{g}}}, \tag{3}$$

where g_{m} and C_{g} denotes the transconductance and the total gate capacitance $C_{\mathrm{g}} = C_{\mathrm{g,int}} + C_{\mathrm{g,par}} + C_{\mathrm{g,ext}}$, respectively, of the device. For f_{T} approximations, the influence of parasitic feed line resistances[2] R_{sd} of source and drain are negligible as long as R_{sd} does not exceed $10k\Omega$. Although resistive parasitics are not analyzed in detail, care must be taken especially regarding the width of the gate fingers. The gate resistance impacts significantly the unilateral power gain frequency $f_{\max}$ due to the small cross sectional area of the gate finger. The total gate resistance can be lowered by using more gate fingers. However, the connection of the gate fingers through feed lines contributes also to the total parasitic resistance.

Both, $C_{\mathrm{g,par}}$ and $C_{\mathrm{g,ext}}$ scale with the number n_{t} of tubes and the number n_{g} of gate fingers. For the feed line parasitics we assume $C_{\mathrm{g,ext}} = n_{\mathrm{g}}\tilde{C}_{\mathrm{g,ext}}$ where $\tilde{C}_{\mathrm{g,ext}}$ is the value for one finger. Most often, due to fabrication constraints, the total gate width w_{g} is longer than $n_{\mathrm{t}}w_{\mathrm{uc}}$. The resulting parasitic overlap capacitance $C_{\mathrm{g,ov}} \approx n_{\mathrm{g}}(w_{\mathrm{g}} - n_{\mathrm{t}}w_{\mathrm{uc}})\bar{C}_{\mathrm{g,uc}}$ contributes to $C_{\mathrm{g,par}}$.

Let $w_{\mathrm{ov}} = w_g - n_{\mathrm{t}}w_{\mathrm{uc}}$ be the gate finger overlap and $n_{\mathrm{ch}} = n_{\mathrm{t}}n_{\mathrm{g}}$ be the total number of channels. Introducing the *gate parasitic scaling factor*

$$\eta_{\mathrm{g}} = 1 + \frac{d_{\mathrm{cc}}}{d_{\mathrm{cnt}}} + \frac{1}{n_{\mathrm{t}}}\frac{w_{\mathrm{ov}}}{d_{\mathrm{cnt}}}, \tag{4}$$

the total parasitic channel capacitance $C_{\mathrm{g,par}}$ reads

$$C_{\mathrm{g,par}} = n_{\mathrm{ch}}\eta_{\mathrm{g}}C^{\min}_{\mathrm{g,uc}}, \tag{5}$$

and the transit frequency reduces to

$$f_{\mathrm{T}} = f_{\mathrm{T,int}}\frac{1}{1 + \eta_{\mathrm{g}}\frac{C^{\min}_{\mathrm{g,uc}}}{C_{\mathrm{g,int}}} + \frac{1}{n_{\mathrm{t}}}\frac{\tilde{C}_{\mathrm{g,ext}}}{C_{\mathrm{g,int}}}}, \tag{6}$$

where $f_{\mathrm{T,int}}$ denotes the intrinsic transit frequency without any parasitics between the contacts. Intrinsic quantities are commonly given by numerical device simulators. Interestingly, η_{g} and $\tilde{C}_{\mathrm{g,ext}}$ are determined by fabrication constraints like the tube separation and by the layout of the feed lines. However, as noted in the last section the minimum parasitic gate capacitance per unit cell $C^{\min}_{\mathrm{g,uc}}$ is especially for un-doped CNTFETs enforced by device specifications[3].

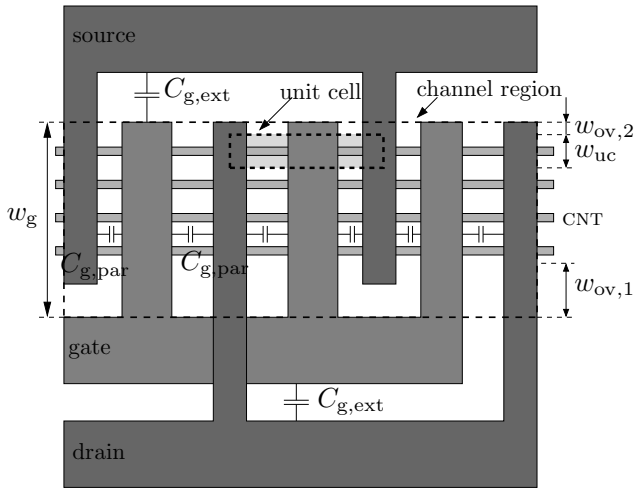

Figure 4: Multi-finger layout of a multi-tube CNTFET. All capacitive parasitics within the bigger dashed box belong to the channel parasitics $C_{\mathrm{g,par}}$ while all parasitics outside of this box belong to $C_{\mathrm{g,ext}}$.

Note, that for a single-tube device $\eta_{\mathrm{g,min}}$ equals one whereas for multi-tube devices $\eta_{\mathrm{g,min}}$ equals three. Since down-scaling of η_{g} is limited to one, $\eta_{\mathrm{g}}C^{\min}_{\mathrm{g,uc}}/C_{\mathrm{g,int}} \ll 1$ and $\tilde{C}_{\mathrm{g,ext}}/(n_{\mathrm{t}}C_{\mathrm{g,int}}) \ll 1$ is needed to profit from the intrinsic high speed capabilities. In this case, the device is operated in the *intrinsic limit* in contrast to the *extrinsic limit*, where at minimum one of the capacitance quotients is much bigger than one. However, especially for un-doped CNTFETs the short gate-source spacer length which ensures high current densities can push the gate capacitance quotient $C^{\min}_{\mathrm{g,uc}}/C_{\mathrm{g,int}}$ close to one.

For the given device, the intrinsic gate capacitance $C_{\mathrm{g,int}}$ is around $0.5a$F over a wide bias range. Hence, $C^{\min}_{\mathrm{g,uc}}/C_{\mathrm{g,int}}$ equals 0.13 for a diameter of $d_{\mathrm{cnt}} = 1.6n$m.

To get a feeling for the layout impact, both layout limits, the single-tube and the single-gate finger layout are studied below. The external capacitance per finger $\tilde{C}_{\mathrm{g,ext}}$ is assumed to be $100a$F which seems to be realizable with current technologies. Fig. 5 shows the dependence of the transit frequency on n_{ch} and d_{cc} for the single-tube and the single-finger layout.

[2]With the dimensions listed above and assuming a maximum R_{sd} of $10k\Omega$, the total drain and source feed line length should not exceed 20μm if Palladium contacts with a resistivity of $105n\Omega\,n$m are used.

[3]Due to the discreteness of the active channel it is worth to scale $C_{\mathrm{g,uc}}$ with d_{cnt} instead of dealing with a capacitance $\bar{C}_{\mathrm{g,uc}}$ per length.

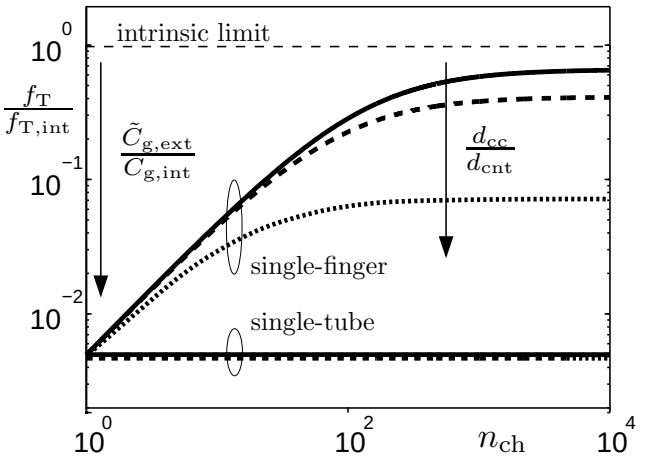

Figure 5: Impact of the channel number n_{ch} on the transit frequency f_{T} for a single-finger and a single-tube layout. The tube separation factor is varied $(3, 10, 100)$.

For a *single-tube layout*, the RF device behavior strongly depends on $\tilde{C}_{\mathrm{g,ov}} = C_{\mathrm{g,ov}}/n_{\mathrm{g}}$ and $\tilde{C}_{\mathrm{g,ext}}$. For our PA example, 100 gate fingers are needed. Even if $w_{\mathrm{ov}} = 0$, the transit frequency f_{T} drops already to $0.005 f_{\mathrm{T,int}}$ $(40G\mathrm{Hz})$. Taking additionally $\tilde{C}_{\mathrm{g,ov}}$ into account, the single-tube layout is noncompetitive.

For a *single gate-finger layout* with 100 tubes in parallel, however, $\tilde{C}_{\mathrm{g,ov}}$ and $\tilde{C}_{\mathrm{g,ext}}$ decrease with the number of tubes and the tube separation d_{cc} becomes important. To ensure in our example an $f_{\mathrm{T}} \approx 2T\mathrm{Hz}$ the tube separation factor $d_{\mathrm{cc}}/d_{\mathrm{cnt}}$ should not exceed 10 which is close to minimum η_g and $C_{\mathrm{g,ov}}/C_{\mathrm{g,int}}$ is limited approximately to the tube number.

As mentioned above, a compromise between the number of tubes in parallel and the number of gate-fingers has to be found in a *multi-finger layout*, to achieve f_{T} values comparable to $f_{\mathrm{T,int}}$.

5 RESULTS AND DISCUSSION

In this work, we proposed a CNTFET device design suitable for analog circuit design, i. e., with a fairly large $V_{\mathrm{dc,max}}$, high saturation current and very high intrinsic transit frequency. To enable the circuit designer using the fundamental intrinsic RF device capabilities, different layout optimization guidelines depending on a given technology were presented. In general, external parasitics and overlap parasitics can be minimized if the channel number is increased either by more tubes in parallel or by more gate fingers. For high channel numbers, a multi-tube technology should be preferred compared to a single-tube technology. So far, we used a ballistic transport model. However, especially for high bias the scattering rate could increase significantly owing to a charge pile up [10] in the tube which lowers the transit frequency. To further improve the optimization results, f_{max} has to be included in future layout optimizations.

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