High-Voltage MOSFET Model Valid for Device Optimization

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ABSTRACT

We have developed the high-power MOSFET model HiSIM_HV based on the complete surface-potential-based description. It is demonstrated here that HiSIM_HV is suitable even for device optimization.

Keywords: high-voltage, surface potential, ldmos, compact model

1 INTRODUCTION

Requirement for high performance circuits with power devices are expanding due to the global warming problem. This is because the power devices play an important role for operation high power efficiently. It is believed that the MOSFET based power devices continue to be important in future. For this purpose, accurate compact models of the high-voltage MOSFETs are highly required. However, developing compact models for the devices are not easy task due to complicated carrier dynamics within the device. Recently HiSIM_HV has been selected as the standard model by the Compact Model Council (CMC) due to its elevated features in comparison to existing models. Here we extend the model to be applicable even for device optimization.

2 MODELING OF HV-MOSFET

The most successfully applied MOSFET model is BSIM based on the threshold voltage [1]. A big advantage of the modeling approach is that electric characteristics of the MOSFET are written directly as a function of applied biases [2]. However, it has been realized that the description derived by the potential pinning within the MOSFET is no more accurate enough for advanced MOSFETs. Thus the surface-potential-based modeling approach, solving the Poisson equation explicitly for calculating the potential distribution, is getting more familiar. It is shown here that this approach is exactly profitable for developing the high-voltage MOSFET models, requiring the potential distribution along the channel down to the drain contact into the consideration.

A conventional MOSFET modeling is done by solving the Poisson equation under two approximations: One is the gradual-channel approximation, considering only the gradual potential increase along the device, and the other is the surface-potential approximation, considering that the channel charge is located only at the surface. Under these approximations all device characteristics are described as a function of two surface potentials, ϕ_{S0} and ϕ_{SL} as schematically shown in Fig. 1 [3]. The Poisson equation is solved at source side and drain side independently with the quasi-Fermi potential. HiSIM considers further potential increase beyond the pinch-off point, thus providing the complete potential distribution along the channel down to drain.

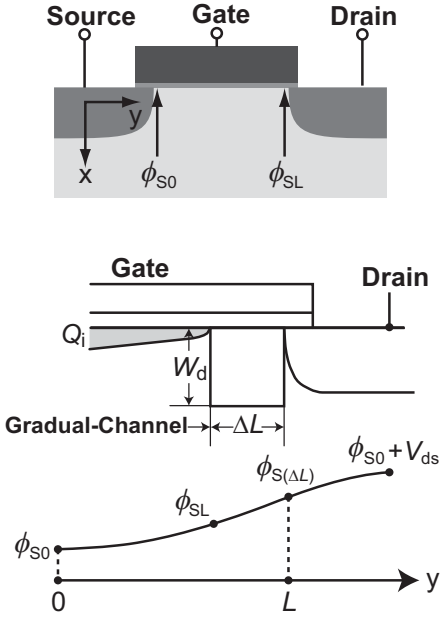


Fig. 1. Surface-potential distribution along the device, which is considered in HiSIM.

HiSIM_HV is based on the complete surface-potential-based concept as shown schematically in Fig. 1 [4, 5]. The major potential drop is absorbed in a high resistive region, called the drift region. This resistive drift region causes specific features of power MOSFETs such as the quasi-saturation and anomalous characteristics in capacitances. Thus the most effort has been given on modeling of the resistance effect in the drift region. The device parameters, which determine the resistance in the drift region, are the length and the impurity concentration. In HiSIM_HV the resistance effect is solved in the form

$$\Delta V = I_{ds} \times R_d \quad (1)$$

where R_d is a function of device parameters in the drift region as well as of applied voltages. For high frequency applications the Eq. (1) includes additional terms, which is neglected here for simplicity. It is obvious that Eq. (1) can be solved only iteratively, because the potential drop ΔV must be known to calculate I_{ds}, and I_{ds} itself is a function of the internal node potential at the end of the channel. Iteration can be done within HiSIM_HV by a flowchart as shown in Fig. 2. However, it is also possible to introduce the independent internal node (at the position L in Fig. 1), and let circuit simulator solve the potential node.

The simulated potential values at the internal node potential $\phi_{s(\Delta L)}$ with a 2D-device simulator are compared in Fig. 3. The feature is that the potential increase is strongly suppressed by the resistance effect. Fig. 4 compares with HiSIM_HV results. The anomalous potential characteristics are the origin of all observed LDMOS-MOSFET features. However, as ΔV in the source dominates, these anomalies disappear in the symmetrical HV-MOSFET.

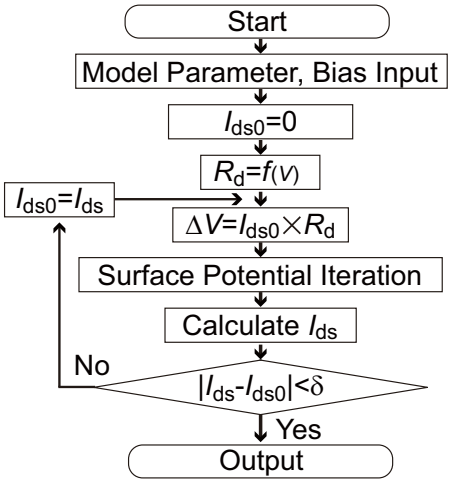
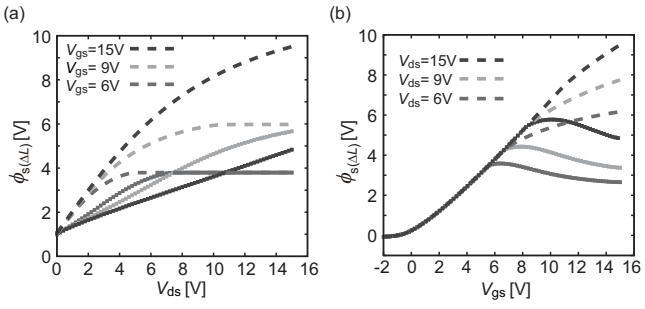


Fig. 2. Flowchart how to solve the resistance effect within a model.



Figs. 3. Potential values on the internal node as a function of (a) V_{gs} and (b) V_{ds}. Solid lines are with the resistance effect and dashed lines are without.

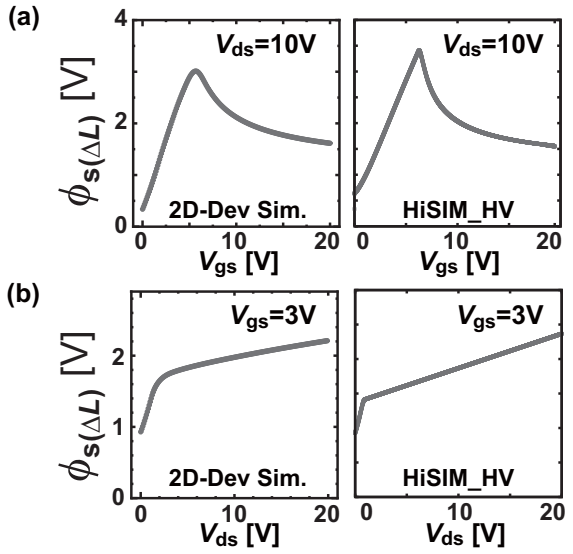


Fig. 4. Potential values at the channel/drift junction $\phi_{s(\Delta L)}$ as a function of gate voltage V_{gs} and drain voltage V_{ds} in comparison to 2D-device simulation results.

3 DEVICE OPTIMIZATION

Fig. 5 shows the schematic LDMOS structure, an asymmetrical HV-MOS. Usually the drift region length L_{drif} and the overlap length L_{over} are optimized to realize required device performances. Fig. 6 shows 2D-device simulation results of the drain current I_{ds} with elongated L_{drif} and L_{over} lengths. Symbols show results with nominal lengths of L_{drif}=2μm and L_{over}=1μm. Results with elongated lengths are depicted by lines. Reduction of I_{ds} is obvious at the transition region from the linear to the saturation condition for the longer L_{drif} length. On the contrary, I_{ds} enhancement is observed for the increased L_{over} length. Though long L_{drif} results in the increased resistance effect, long L_{over} suppresses the resistance effect.

HiSIM_HV describes the resistance as a function of applied voltages

$$R_d \propto \mathbf{RD} + V_{ds} \times \mathbf{RDVD} \quad (2)$$

where **RD** and **RDVD** are model parameters. The resistance effect is modified by the accumulated carrier concentration underneath the overlap region. The potential increase occurs, resulting in the reduction of the resistance effect in the drift region. This is considered in the resistance model as a function of the gate voltage V_{gs}.

Fig. 7 shows comparison of calculated HiSIM_HV results with 2D-device simulation results. Fig. 8 compares the case shown in Fig. 6a, and Fig. 9 shown in Fig. 6b. Fig. 10 shows extracted resistance as a function of the drift length L_{drif}. Fig. 11 shows extracted resistance as a function of L_{over}. For both cases the effect becomes larger for larger applied biases.

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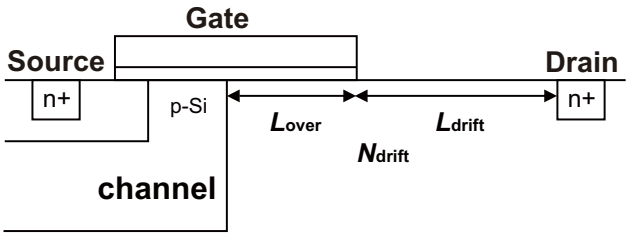

Fig. 5. Device parameters considered in high-voltage MOSFETs.

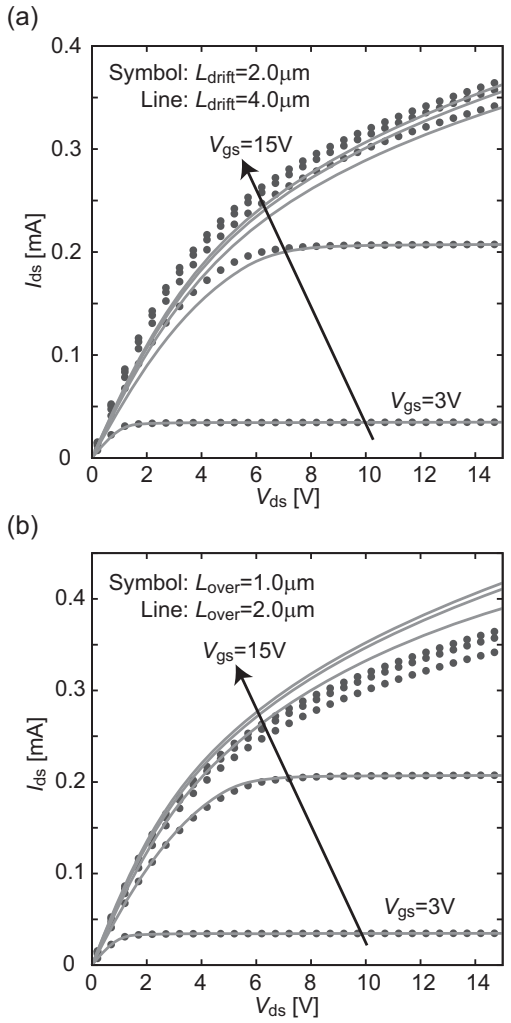

Fig. 6. Comparison of 2D-device simulation results of the drain current I_{ds} as a function of the drain voltage V_{ds}, (a) for different L_{drif} lengths, and (b) for different L_{over} lengths. Symbols are simulation results with nominal lengths and lines are those with elongated lengths.

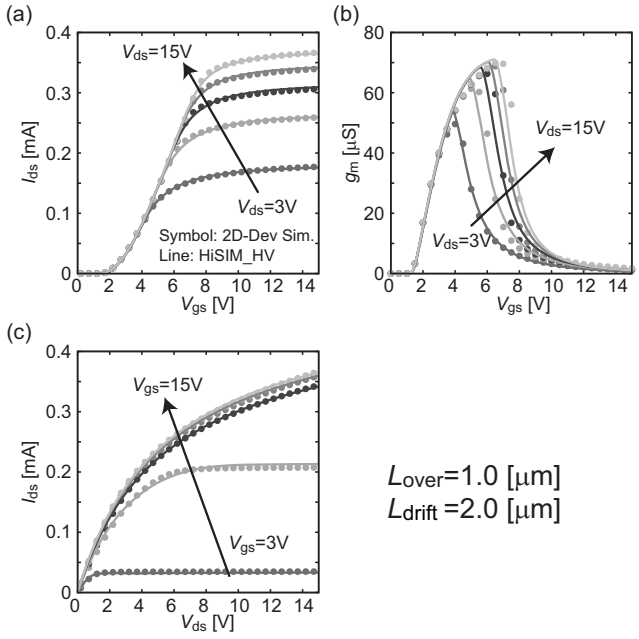

Fig. 7. Comparison of HiSIM_HV calculation results of the drain current I_{ds} with 2D-device simulation results. Lines are HiSIM results and Symbols are 2D-device simulation results.

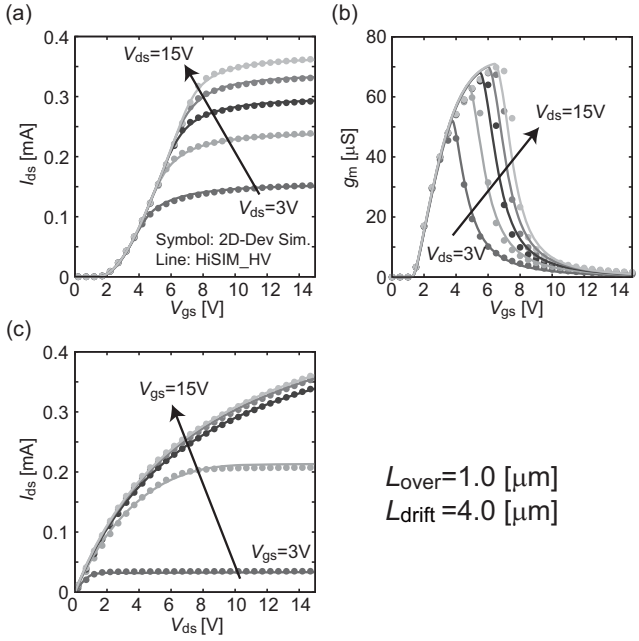

Fig. 8. The same comparison as shown in Fig. 7 with different drift length L_{drif}.

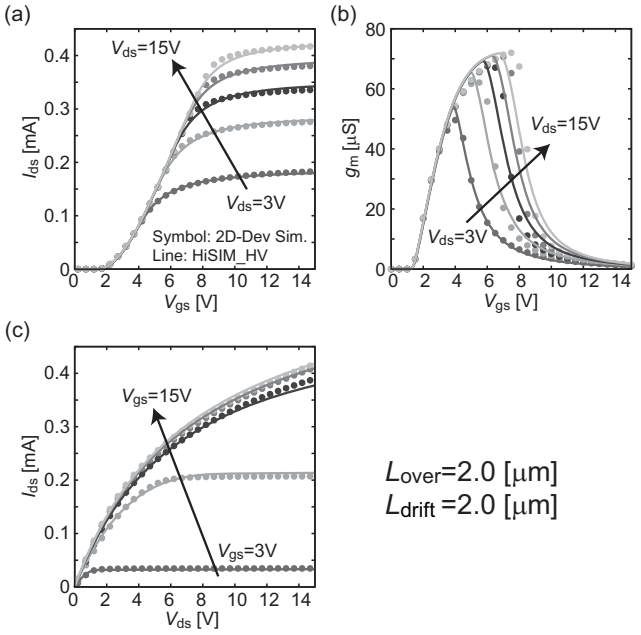

Fig. 9. The same comparison as shown in Fig. 7 with different overlap length L_{over}.

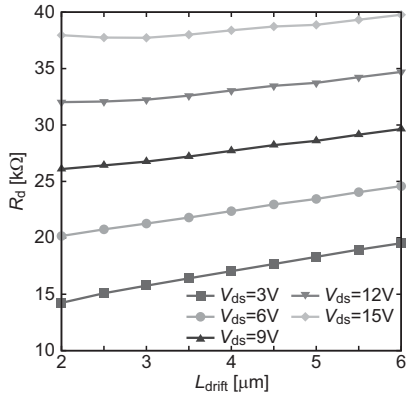

Fig. 10. Extracted resistance in the drift region R_d as a function of the drift length L_{drift}.

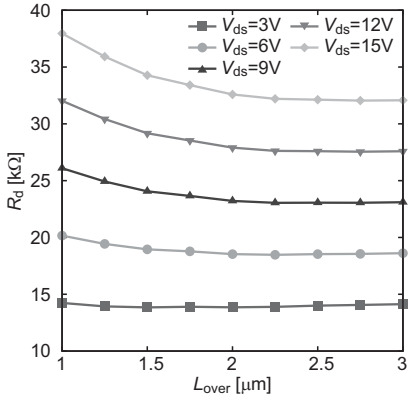

Fig. 11. Extracted resistance in the drift region R_d as a function of the overlap length L_{over}.

4 CONCLUSION

We have developed the high-power MOSFET model HiSIM_HV based on the complete surface-potential-based description. The dependence of the resistance in the drift region on the device structure and bias condition is analyzed. It is demonstrated here that the developed model HiSIM_HV is applicable for device optimization.

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