Simulation of Decrease in Lag Phenomena and Current Slump of Field-Plate GaAs FETs

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ABSTRACT

Two-dimensional simulation of GaAs MESFETs with a field plate is performed in which a deep donor "EL2" is considered in a semi-insulating substrate. It is studied how the existence of field plate affects substrate-related lag phenomena and current slump. It is shown that the drain lag and current slump could be reduced by introducing a field plate, because electron trapping in the substrate is weakened by it. Dependence of lag phenomena and current slump on the field-plate length and on the insulator thickness under the field plate is also studied. It is suggested that there are optimum values for the field-plate length and insulator thickness to reduce the current slump and also to maintain the high frequency performance of GaAs FETs.

Keywords: GaAs, FET, drain lag, current slump, trap

1 INTRODUCTION

In compound semiconductor FETs, slow current transients are often observed even if the gate voltage or the drain voltage is changed abruptly [1]. This is called gate lag or drain lag, and is problematic for circuit applications. The slow transients mean that dc *I-V* curves and RF *I-V* curves become quite different, resulting in lower RF power available than that expected from dc operation [2]. This is called power slump or current slump. These are serious problems, and many experimental works are reported [1-6], and some theoretical works are made [6-8]. The lags and current slump can be reduced by surface passivation [3] and by using a field plate [4,5]. This is considered due to the decrease in surface-state effects. However, up to now, few simulation works on the field plate structure have been reported. Therefore, in this work, we have made simulations of field-plate GaAs MESFETs with a semi-insulating substrate and found that substrate-related lag phenomena and current slump could be reduced by introducing a field plate.

2 PHYSICAL MODEL

Figure 1 shows a device structure simulated in this study. The gate length L_G is typically set to 0.3 μm. The gate electrode extends on to SiO_2 passivation layer. This is called a field plate. The field-plate length L_{FP} is varied as a parameter. The thickness of SiO_2 layer d is also varied. As a substrate, we consider undoped semi-insulating GaAs where deep donors "EL2" (N_{EL2}) compensate shallow acceptors (N_{Ai}) [9]. The energy level of EL2 is set to 0.69 eV below the bottom of conduction band, and its capture cross-sections for electrons and holes are set to 4.68×10^{-16} cm^2 and 2×10^{-18} cm^2, respectively, at T = 300 K [10]. We also assume N_{Ai}/N_{EL2} = 0.1, which corresponds to an equilibrium electron density of 10^7 cm^{-3} in the substrate. EL2 usually acts as an electron trap.

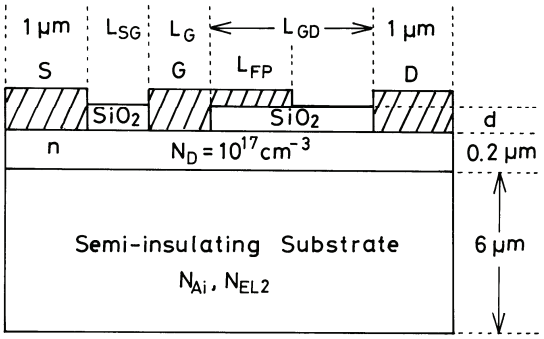

Figure 1: Device structures simulated in this study.

Basic equations to be solved are Poisson's equation including an ionized deep-level term, continuity equations for electrons and holes which include carrier loss rates via the deep level and a rate equation for the deep level. These are expressed as follows.

1) Poisson's equation

$$\nabla^2\psi = -\frac{q}{\varepsilon}(p - n + N_D - N_{Ai} + N^+_{EL2}) \tag{1}$$

2) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - R_{n,EL2} \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \bullet J_p - R_{p,EL2} \tag{3}$$

where

$$R_{n,EL2} = C_{n,EL2}N^+_{EL2}n - e_{n,EL2}(N_{EL2} - N^+_{EL2}) \tag{4}$$

$$R_{p,EL2} = C_{p,EL2}(N_{EL2} - N^+_{EL2})p - e_{p,EL2}N^+_{EL2} \tag{5}$$

3) Rate equation for the deep level

$$\frac{\partial}{\partial t}(N_{\mathrm{EL2}} - N_{\mathrm{EL2}}^{+}) = R_{n,\mathrm{EL2}} - R_{p,\mathrm{EL2}} \qquad (6)$$

where N_{EL2}^{+} represents the ionized density of deep donor "EL2". $C_{n,EL2}$ and $C_{p,EL2}$ are the electron and hole capture coefficients of EL2, respectively, $e_{n,EL2}$ and $e_{p,EL2}$ are the electron and hole emission rates of EL2, respectively.

The above basic equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage V_D and/or the gate voltage V_G are changed abruptly.

3 DRAIN LAG

Figure 2 shows calculated drain-current responses of GaAs MESFETs when V_D is lowered abruptly from 10 V to V_{Dfin}, where V_G is kept constant at 0 V. Fig.2(a) is for a structure without a field plate (L_{FP} = 0) and Fig.2(b) is for a case with a field plate (L_{FP} = 1 μm). Here the thickness of SiO_2 passivation layer d is 0.1 μm. In both cases, the drain currents remain at low values for some periods and begin to increase slowly, showing drain-lag behavior. It is understood that the drain currents begin to increase when the deep donors "EL2" in the substrate begin to emit electrons. It is seen that the change of drain current is smaller for the case with a field plate, indicating that the drain lag is smaller for the field-plate structure. We will discuss below why this reduction in drain lag arises.

Figure 3 shows (a) electron density profiles and (b) ionized deep-donor density N_{EL2}^{+} profiles at V_G = 0 V and V_D = 10 V. The left is for the structure without a field plate, and the right is for the field-plate structure. In Fig.3(a), it is seen that for the structure without a field plate, electrons are injected deeper into the buffer layer under the gate, particularly under the drain edge of the gate region. These electrons are captured by the deep donors, and hence N_{EL2}^{+} decreases there as seen in Fig.3(b). As mentioned before, when V_D is lowered abruptly, the drain current remains at a low value for some periods and begins to increase slowly as the deep donors begin to emit electrons (and N_{EL2}^{+} increases), showing drain lag. This electron emission occurs because the state of higher V_D is a state where more electrons are injected into the substrate and captured by EL2, leading to the more negatively charged substrate. In the case of field-plate structure, as seen in Fig.3(a), electrons are injected into the buffer layer under the drain edge of field plate as well as under the gate. But the injection depth is not so deep as compared to the case without a field plate. This is because the electric field at the drain edge of the gate becomes weaker by introducing a field plate. Hence, the change of N_{DD}^{+} by capturing electrons is smaller for the field-plate structure as seen in Fig.3(b). Therefore, the drain lag becomes smaller for the structure with a field plate.

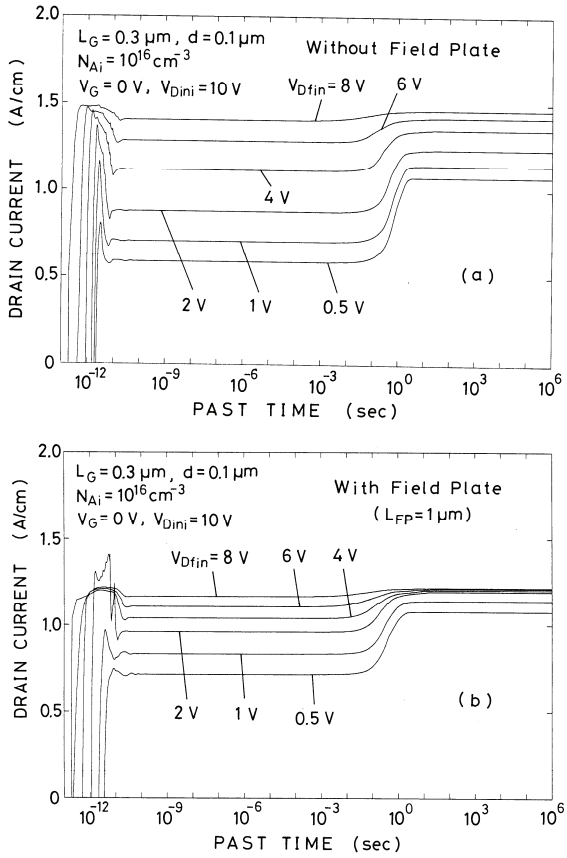

Figure 2: Calculated drain-current responses of GaAs MESFETs when V_D is changed abruptly from 10 V to V_{Dfin}, while V_G is kept constant at 0 V. N_{EL2} = 10^{17} cm^{-3}, N_{Ai} = 10^{16} cm^{-3}. (a) Without field plate, (b) with field plate.

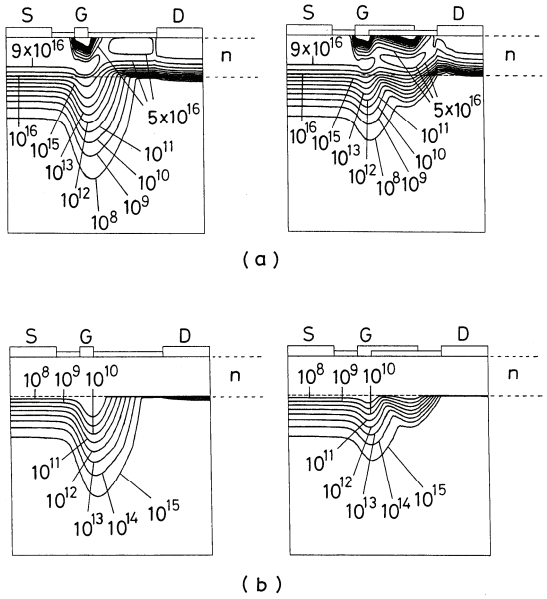

Figure 3: (a) Electron density profiles and (b) ionized deep-donor density N_{EL2}^{+} profiles at V_G = 0 V and V_D = 10 V. d = 0.1 μm. N_{DD} = 10^{17} cm^{-3}, N_{Ai} = 10^{16} cm^{-3}. The left is for the case without field plate, and the right is for the field-plate structure (L_{FP} = 1 μm).

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4 CURRENT SLUMP

Next, we have calculated a case when V_G is also changed from an off point. V_G is changed from the threshold voltage V_{th} to 0 V, and V_D is changed from 10 V to V_{Don} (on-state drain voltage). The characteristics become similar to those in Fig.2, although some transients arise when only V_G is changed (gate lag). From these turn-on characteristics, we obtain a quasi-pulsed *I-V* curve.

In Fig.4, we plot by (x) the drain current at $t = 10^{-8}$ s after V_G is switched on. Fig.4(a) is for the structure without a field plate and Fig.4(b) is for the field-plate structure (L_{FP} = 1 μm). These curves are regarded as quasi-pulsed *I-V* curves with pulse width of 10^{-8} s. They stay rather lower than the steady-state *I-V* curves (solid lines), indicating current slump behavior. In Fig.4, we also plot another pulsed *I-V* curve (Δ), which is obtained from figures like Fig.2 (where only V_D is changed), indicating drain-lag behavior. Note that the gate lag is small in this case. From Fig.4, we can definitely say that the drain lag and current slump become smaller for the structure with a field plate.

5 FIELD-PLATE LENGTH AND INSULATOR THICKNESS DEPENDENCE

We have next studied dependence of lag phenomena and current slump on the field plate length L_{FP} and on the SiO_2 thickness *d*.

Figure 5 shows drain-current reduction rate $\Delta I_D/I_D$ (ΔI_D : current reduction, I_D : steady-state current) due to current slump, drain lag or gate lag, with L_{FP} as a parameter. As L_{FP} becomes longer, the drain lag and current slump become smaller. This can be easily understood because the substrate trapping effects should become smaller for longer L_{FP}.

Figure 6 shows the drain-current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag, with *d* as a parameter. Here $d = 0$ (L_{FP} = 1 μm) corresponds to a case of L_G = 1.3 μm without a field plate. When *d* is thick, the current slump and lag phenomena are relatively large because the field plate does not almost affect the characteristics. As *d* becomes thinner, the current slump and lag phenomena become smaller. This is because the substrate trapping effects are reduced as described in section 3. When $d = 0$ (L_G = 1.3 μm), that is, without a field plate, the current slump becomes rather noticeable.

From Figs.5 and 6, it can be said that to minimize the current slump and drain lag in the field-plate GaAs MESFETs, L_{FP} should be longer and *d* should be thinner. However, when L_{FP} is long and *d* is thin, the gate capacitance becomes large and the high frequency characteristics may degrade. Therefore, it is concluded that there are optimum values of L_{FP} and *d* to reduce the substrate-related current slump and also to maintain the high frequency performance of GaAs FETs.

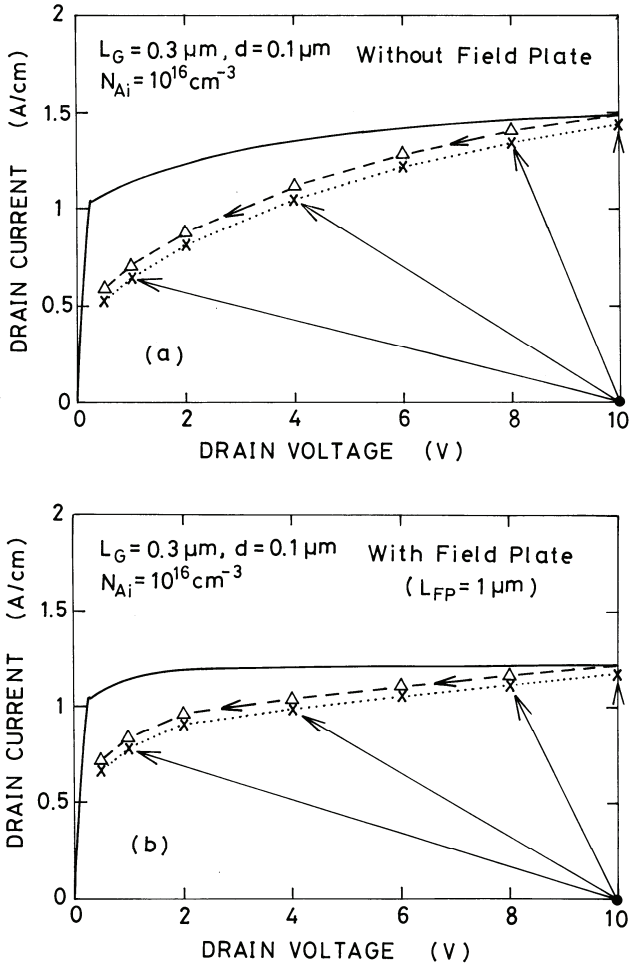

Figure 4: Steady-state *I-V* curves (V_G = 0 V; solid lines) and quasi-pulsed *I-V* curves (Δ, x) of GaAs MESFETs. (a) without field plate, (b) with 1 μm-length field plate. (Δ): Only V_D is changed from 10V ($t = 10^{-8}$ s), (x): V_D is lowered from 10 V and V_G is changed from V_{th} to 0 V ($t = 10^{-8}$ s).

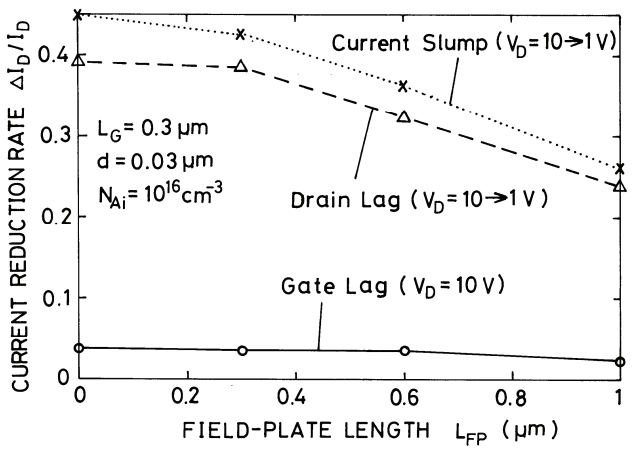

Figure 5: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with field plate length L_{FP} as a parameter. d = 0.03 μm.

6 CONCLUSION

Two-dimensional transient simulations of the field-plate GaAs MESFETS have been performed in which a deep donor "EL2" and a shallow acceptor are considered in the semi-insulating substrate. Quasi-pulsed *I-V* curves have been derived from the transient characteristics. It has been shown that the drain lag and current slump are reduced by introducing a field plate because the electron injection into the substrate is reduced and the trapping effects by the deep donors "EL2" become smaller. It has also been shown that the current slump is smaller for longer field-plate length and for thinner SiO_2 thickness, although in such cases, the gate capacitance should increase and the high-frequency performance may degrade. Therefore, it is concluded that there are optimum values for the field plate length and SiO_2 layer thickness to reduce the current slump and also to maintain the high frequency performance of GaAs FETs.

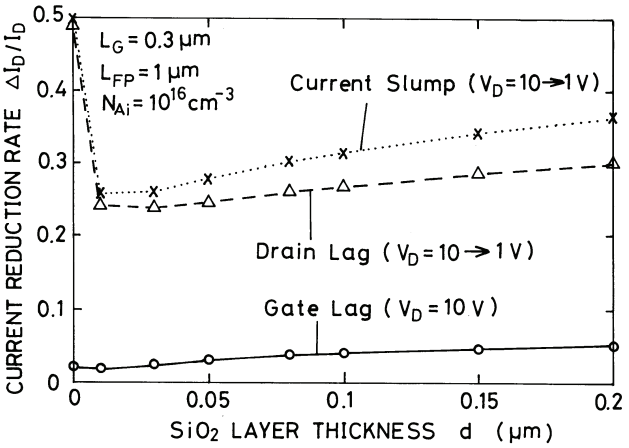

Figure 6: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with SiO_2 thickness d as a parameter. L_{FP} = 1 μm.

REFERENCES

[1] S. C. Binari, P. B. Klein and T. E. Kazior, "Trapping effects in GaN and SiC Microwave FETs", Proc. IEEE, vol.90, pp.1048-1058, 2002.

[2] U. K. Mishra, L. Shen, T. E. Kazior and Y.-F. Wu, "GaN-based RF power devices and amplifiers", Proc. IEEE, vol.96, pp.287-305, 2008.

[3] G. Koley, V. Tilak, L. F. Eastman and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: Effects of SiN*x* passivation and UV illumination", IEEE Trans. Electron Devices, vol.50, pp.886-893, 2003.

[4] A. Wakejima, K. Ota, K. Matsunaga and M. Kuzuhara, "A GaAs-based field-modulating plate HFET with improved WCDMA peak-output-power characteristics", IEEE Trans. Electron Devices, vol.50, pp.1983-1987, 2003.

[5] A. Koudymov, V. Adivarahan, J, Yang, G. Simon and M. A. Khan, "Mechanism of current collapse removal in field-plated nitride HFETs", IEEE Electron Device Lett., vol.26, pp.704-706, 2005.

[6] J. Tirado, J. L. Sanchez-Rojas and J. I. Izpura, "Trapping Effects in the transient response of AlGaN/GaN HEMT devices", IEEE Trans. Electron Devices, vol.54, pp.410-417, 2007.

[7] K. Horio, K. Yonemoto, H. Takayanagi and H. Nakano, "Physics-based simulation of buffer-trapping effects on slow current transients and current collapse in GaN field effect transistors" J. Appl. Phys., vol.98, pp.124502-1–124502-7, 2005.

[8] K. Horio and A. Nakajima, "Physical mechanism of buffer-related current transients and current slump in AlGaN/GaN high electron mobility transistors", Jpn. J. Appl. Phys., vol.47, 2008.

[9] Y. Kazami, D. Kasai and K. Horio, "Numerical analysis of slow current transients and power compression in GaAs FETs", IEEE Trans. Electron Devices, vol.51, pp.1760-1764, 2004.

[10] K. Horio, A. Wakabayashi and T. Yamada, "Two-dimensional analysis of substrate-trap effects on turn-on characteristics in GaAs MESFET's", IEEE Trans. Electron Devices, vol.47, pp.617-624, 2000.

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