HiSIM-SOI: SOI-MOSFET Model for Circuit Simulation Valid also for Device Optimization

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ABSTRACT

Circuit simulation model for advanced SOI-MOSFETs has been developed by solving Poisson's equation consistently. It is successfully proven that, as a result of solving the Poisson's equation considering its device structure, our model is applicable for various variations of SOI-MOSFETs such as partially depleted (PD), fully depleted (FD) and dynamically depleted SOI-MOSFETs, which is the indispensible feature as a compact model to be applied for device optimization. Floating body effect is also reproduced by considering the accumulated holes within SOI body region, which is included in the Poisson's equation, confirming the advantages of the potential based modeling.

1. INTRODUCTION

SOI-MOSFETs are considered to be suitable for high performance circuits as well as low power applications due to their improved driving capability and reduced junction capacitances [1, 2]. The development trend approaches toward the thinner SOI films to enhance the device characteristics. This trend seems to take steps toward the ultimate MOSFET structure, namely the DG-MOSFET structure [3, 4]. Thus the requirement for compact models is to cover all such development steps and to predict the device characteristics. To satisfy this requirement, we have developed HiSIM-SOI based on the frame work of the surface potential based model HiSIM, to make it possible to predict device characteristics from its structural device parameters for the device development.

2. MODEL CONCEPT OF HiSIM

HiSIM is a compact circuit simulation model based on the complete surface-potential description, which is obtained from the Poisson equation solved iteratively at the source and drain end considering gradual channel and sheet channel approximation, as shown in figure 1. The calculated potential values determine all device characteristics consistently [5, 6, 7], this method guarantees consistency among calculated device characteristics. This concept is applied to HiSIM-SOI by extending the Poisson equation.

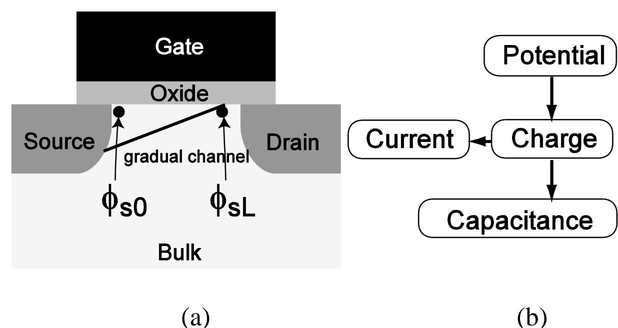

Fig. 1. Basic concept of HiSIM (a) 2 surface potentials solved in HiSIM and (b) calculation flow

3. CORE MODELING OF SOI-MOSFET

As compared with conventional bulk MOSFETs, SOI-MOSFETs have an additional oxide in the substrate (BOX), in HiSIM-SOI not only the surface potential at the front gate oxide (FOX) interface, but also 2 additional potential values must be calculated as show in fig. 2 and resulting Poisson's equation solved in HiSIM-SOI is shown below considering all possible charges which will be induced within SOI-MOSFET [8,9].

$$V_{gs} - V_{fb} - \Delta V_{th} = \phi_{s.SOI} - \frac{Q_i + Q_{dep} + Q_{b.SOI} + Q_{s.bulk}}{C_{FOX}}$$

$$\phi_{b.SOI} = \phi_{s.bulk} - \frac{Q_{s.bulk}}{C_{BOX}} \qquad (1)$$

$$\phi_{s.SOI} = \phi_{b.SOI} - \frac{Q_{s.bulk} + \frac{1}{2} Q_{dep}}{C_{SOI}}$$

here the meaning of each symbols in equation 1 is shown in fig. 2.

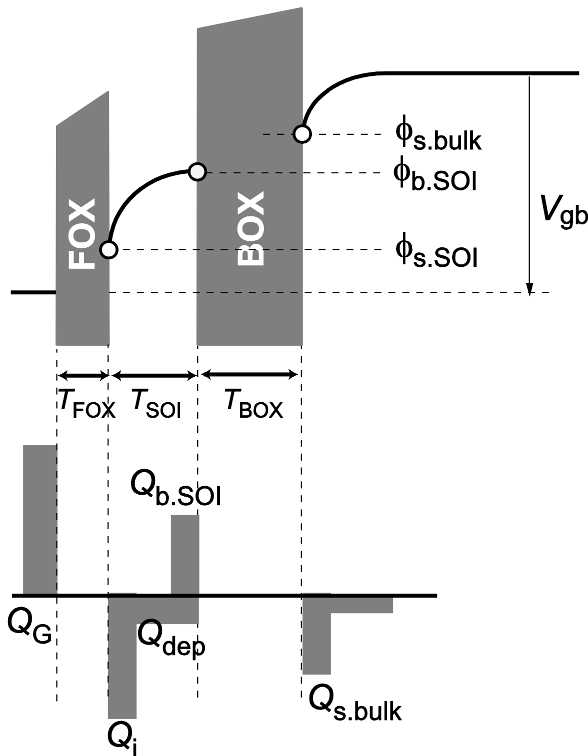

Fig. 2. Schematic band diagram of the SOI-MOSFET and induced charges considered in HiSIM-SOI. 3 potentials solved in HiSIM-SOI are shown by circles.

Calculated 3 potential values are plotted in fig. 3 as compared with 2D TCAD data for 3 different operation regions and 4 different wide ranges of SOI device structures which are summarized in table 1. Calculation results of gate capacitances are plotted in fig. 4. PD device (Device1) shows similar *C-V* curve as conventional bulk-MOSFETs on the other hand, FD device (Device4) have specific capacitance characteristics in depletion region around -0.4<Vg<0 V region due to the fully depleted SOI body. Intermediate behaviors between PD and FD devices are observed for dynamic depletion devices in fig. 3(b) and (c).

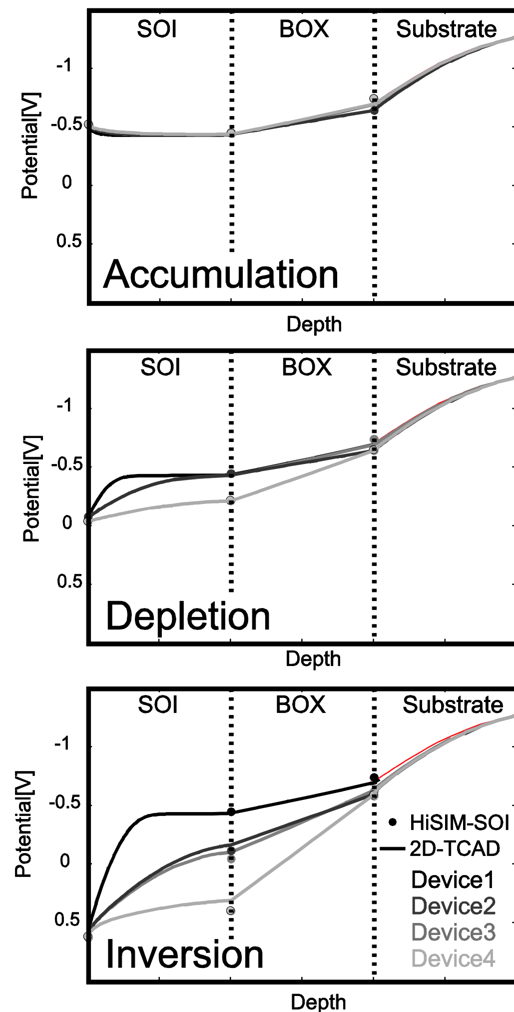

Fig. 3. Calculated surface potential values by HiSIM-SOI for different gate biasing conditions from accumulation to inversion as compared with 2D device simulation results.

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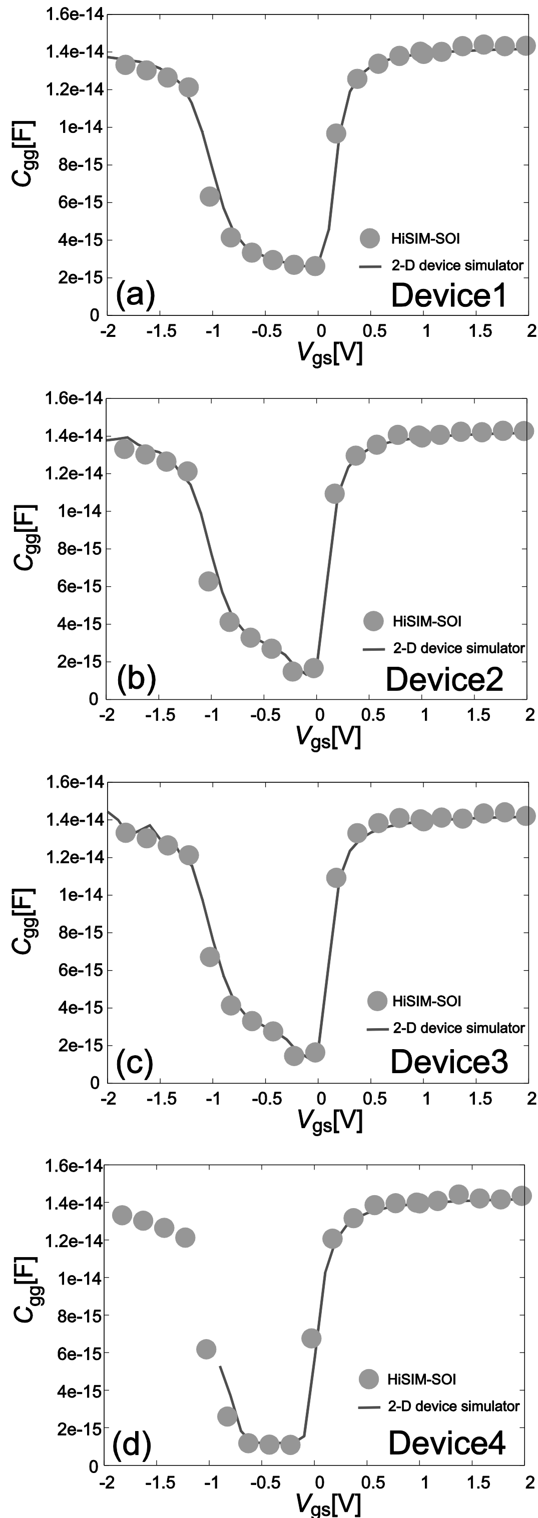

Fig. 4. Calculated gate capacitances as a function of gate voltages for different device structures in table 1. (a) for device1 and (b),(c),(d) for device 2,3,4 respectively. Symbols are result of HiSIM-SOI and lines are results with 2D TCAD simulation.

Table 1. Summary of the device structures investigated in this work. Other device parameters such as front oxide thickness, channel impurity concentrations, gate length, and so on are fixed.

	T_{SOI}	T_{BOX}
Device1	150nm	110nm
Device2	50nm	110nm
Device3	50nm	50nm
Device4	25nm	110nm

4. FLOATING BODY EFFECT MODELING

As is known well, holes which have been generated through the impact ionization accumulates in SOI layer because of the insulating buried oxide as shown in Fig. 5, causing potential value in the SOI body unstable which is called as floating-body effect [10]. This phenomena is also solved in a consistent way by considering accumulated hole charge Q_h in Poisson's equation [11]. Resulting kink current in I_d-V_g curve due to the floating-body effect is depicted in Fig. 6 for different gate biases as compared with 2D TCAD simulation results.

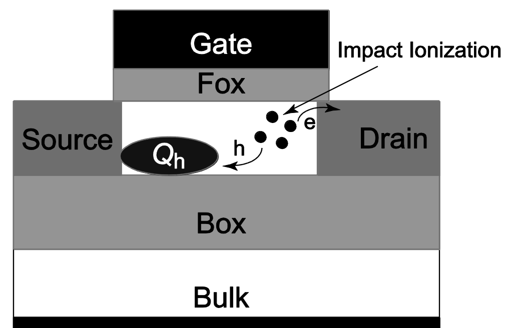

Fig.5. Schematic of accumulated holes in SOI-layer generated by the impact ionization, which cause floating effect in SOI-MOSFETs

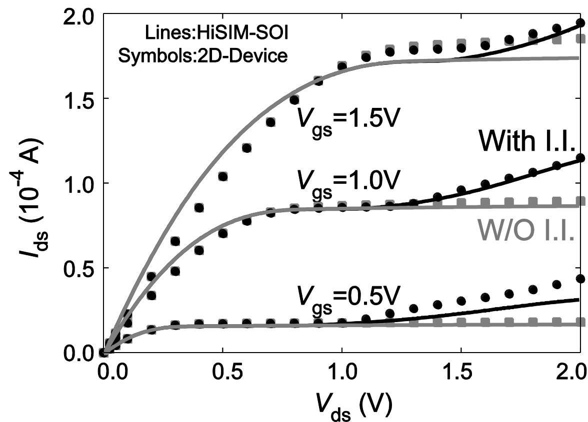

Fig.6. Calculation results of I_d-V_g curve considering floating effect. As a comparison, results without floating body effect are also plotted by a gray lines and symbols.

5. CONCLUSION

Compact circuit simulation model HiSIM-SOI has been developed for advanced SOI-MOSFET. It has been proven that HiSIM-SOI reproduces wide range of SOI structures from PD, FD and DD for all operation regions owing to the exact solution of the Poisson equation. Application to kink current due to the floating body effect reproduction is also presented. This in return means that HiSIM-SOI is applicable for device optimization for SOI developments.

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