SPICE BSIM3 Model Parameters Extraction and Optimization for Low Temperature Application

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ABSTRACT

The SPICE BSIM3v3.1 model parameters extraction and optimization strategy that we present here is applicable for a half micron technology and circuits operating at temperature ranging from -191 to 125^{0}C. The room temperature extraction and optimization strategy [1] is used as basis to extract the temperature dependent BSIM3v3.1 model parameters. The final extracted model parameters accuracy is evaluated by comparing simulations of a 31-stage ring oscillator with measured data.

Keywords: device modeling, MOSFET, parameter extraction, SPICE

1 INTRODUCTION

In this paper we examine BSIM3v3 model parameters extraction and optimization strategy, and its simulation accuracy at low temperature that is above carrier freeze-out. It has been recognized for many years the SPICE model for circuit design at low temperature is needed primarily for space applications of the CMOS ICs and the low temperature effects can also be used as an advantage to improve the speed of circuits. The speed improvement was equivalent to the gain that was achieved from moving towards a next generation in technology. However, the speed improvement of the short channel devices operating at a very low temperature is less than the longer channel devices at the same supply voltage for a given technology because the temperature coefficient of the saturation velocity is smaller compare to the low field mobility [2, 3].

2 MODEL EQUATIONS

In this section the BSIM3v3 temperature effect model equations of the carrier saturation velocity, threshold voltage, source/drain parasitic resistance and carrier mobility are given respectively.

2.1. Carrier Saturation Velocity

In the strong inversion region, the current along the channel of the transistor is given by [4-6].

$$I_{ds} = \mu_{eff} C_{ox} W_{eff} \cdot (V_{gs} - V_{th} - A_{bulk} V_{ds} / 2) \cdot V_{ds} / (L_{eff} + V_{ds} \mu_{eff} / 2 v_{sat}) \quad (1)$$

$$A_{bulk} = \left\{ 1 + \frac{K_1}{2\sqrt{\phi_s - V_{bseff}}} \left\{ \left[\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}} \right] \cdot \left[1 - A_{gs} V_{gst} \left(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}} \right)^2 \right] \right\} + \frac{B_0}{W_{eff} + B_1} \right\} \frac{1}{1 + KETA V_{bseff}} \quad (2)$$

The parameters that represent device channel effective length and width, oxide capacitance, gate voltage, drain/source voltage, substrate bias voltage, junction depth, depletion width, surface potential, and *carriers saturation velocity* are given respectively: L_{eff}, W_{eff}, C_{ox}, V_{gs}, V_{ds}, V_{bs}, X_j, X_{dep}, ϕ_s, v_{sat}.

The *saturation velocity* at temperature *T* is

$$v_{sat}(T) = v_{sat}(T_{nom}) - A_T \left(\frac{T}{T_{nom}} - 1 \right) \quad (3)$$

Where T_{nom}=27^{0}C is the nominal temperature at which the parameters were extracted.

2.2. Threshold Voltage

The *threshold voltage* model in BSIM3v3 is given by

$$\begin{aligned} V_{th} &= V_{th0} + k_1 \left(\sqrt{|\varphi_s - V_{bseff}|} - \sqrt{|\varphi_s|} \right) - k_2 V_{bseff} + \\ & k_1 \left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1 \right) \sqrt{\varphi_s} + (k_3 + k_{3b} V_{bseff}) \frac{T_{ox}}{W_{eff} + W_0} \varphi_s - D_{vt0w} \left[\exp\left(-D_{vt1w} \frac{W_{eff} \cdot L_{eff}}{2 l_{tw}} \right) + \right. \\ & \left. 2 \exp\left(-D_{vt1w} \frac{W_{eff} \cdot L_{eff}}{l_{tw}} \right) \right] (V_{bi} - \varphi_s) - D_{vt0} \left[\exp\left(-D_{vt1} \frac{L_{eff}}{2 l_t} \right) + 2 \exp\left(-D_{vt1} \frac{L_{eff}}{l_t} \right) \right] (V_{bi} - \varphi_s) - \\ & \left[\exp\left(-D_{sub} \frac{L_{eff}}{2 l_{t0}} \right) + 2 \exp\left(-D_{sub} \frac{L_{eff}}{l_{t0}} \right) \right] (Etao + Etab) V_{ds} . \end{aligned} \quad (4)$$

$$V_{th}(T) = V_{th}(T_{nom}) + (K_{T1} + K_{T1L}/L_{eff} + K_{T2}V_{bseff})(\frac{T}{T_{nom}} - 1) \quad (5)$$

2.3. Source/Drain Parasitic Resistance

The model for the *parasitic resistance* is a simple expression using the channel current equation in the linear region:

$$I_{ds} = V_{ds} / R_{tot} = V_{ds} /(R_{ch} + R_{ds}) \quad (6)$$

where parameter R_{ch} is the channel resistance calculated from equation (1) as

$$R_{ch} = [I_{ds} / V_{ds}]^{-1} = \left[\mu_{eff} C_{ox} \frac{W \cdot (V_{gs} - V_{th} - A_{bulk} V_{ds} / 2)}{L + V_{ds}\mu_{eff} / 2v_{sat}}\right]^{-1} \quad (7)$$

where R_{ds} is the *parasitic resistance* given by

$$R_{ds} = R_{\mathrm{dsw}}[1 + P_{rwg}V_{gst} + P_{rwb}(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})]/(10^{-6}W_{eff})^{W_r}. \quad (8)$$

$$R_{dsw}(T) = R_{dsw}(T_{nom}) + P_{RT}(\frac{T}{T_{nom}} - 1) \quad (9)$$

2.4. Carrier Mobility

In this work the carrier mobility SPICE model option MOBMOD=1 is used:

$$\mu_{eff} = \frac{\mu_0}{1 + (U_a + U_c \cdot V_{bseff})(\frac{V_{gst} + 2V_{th}}{T_{ox}}) + U_b(\frac{V_{gst} + 2V_{th}}{T_{ox}})^2} \quad (10)$$

and

$$V_{gst} = \frac{2n \cdot v_t \ln[1 + \exp(\frac{V_{gs} - V_{th}}{2n \cdot v_t})]}{1 + 2n \cdot Cox\sqrt{\frac{2\phi_s}{q\varepsilon_{si}N_{ch}}}\exp(\frac{-V_{gs} + V_{th} + 2V_{off}}{2n \cdot v_t})}$$

Where v_t is the thermal voltage, q is the charge and μ_0 is the parameter which represents the low field mobility (ideal mobility of a large device.) The coefficients U_a, U_b and U_c are parameters that represent the reduction of the channel mobility by the vertical field.

$$\mu_0(T) = \mu_0(T_{nom})(\frac{T}{T_{nom}})^{U_{TE}} \quad (11)$$

$$U_i(T) = U_i(T_{nom}) + U_{i1}(\frac{T}{T_{nom}} - 1) \quad (12)$$

where *i=a, b and c.*

3 PARAMETER EXTRACTION AND OPTIMIZATION STRATEGIES

The room temperature extraction and optimization strategy [1] is used as basis to extract the temperature dependent BSIM3v3.1 model parameters. The strategies listed below are used for optimization of the temperature parameters and the I-V data which are different to the room temperature should be used. In our case we used the data measured at T= -191^{0}C.

Strategy 1: (Threshold and mobility parameters without body bias effect)
This local strategy is applied for wide and long device only, and the parameters are those in equation (5), (11) and (12).
Target parameters: K_{T1}, U_{TE}, U_{A1} and U_{B1}.
It requires I_{ds} versus V_{gs} data with low V_{ds} and varying V_{bs}.

Strategy 2: (Threshold and mobility parameters with body bias effect)
This local strategy is applied for wide and long device only, and the parameters are those in equation (5) and (12).
Target parameters: K_{T2} and U_{C1}.
It requires I_{ds} versus V_{gs} data with low V_{ds} and varying V_{bs}.

Strategy 3: (Threshold and channel resistance parameters)
This local strategy is applied for wide and short device, and the parameters are those in equation (5) and (9).
Target parameters: K_{T1L} *and* P_{RT}
It requires I_{ds} versus V_{gs} data with low V_{ds} and varying V_{bs}.

Strategy 4: (Low Bias Drain Saturated Current Parameters.)
This local optimization strategy uses only short channel devices and the temperature parameter in equation (3) is optimized.
Target parameter: A_T.
It requires I_{ds} versus V_{ds} data with low V_{bs} and varying V_{gs}.

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4 RESULTS AND DISCUSSIONS

The HSPICE model cards in Table 1 and Table 2 are generated for 0.5 micron technology using the above extraction and optimization strategies.

```
* W_min =2.4µm and L_min =0.6µm
* Temperature_parameters=optimized
.MODEL CMOSN NMOS (                     LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 1.39E-8
+XJ     = 1.5E-7        NCH     = 1.7E17      VTH0    = 0.719346
+K1     = 0.9504347     K2      = -0.1223091  K3      = 32.8194652
+K3B    = -18.2798187   W0      = 6.962875E-7 NLX     = 1E-9
+DVT0W  = 0             DVT1W   = 0           DVT2W   = 0
+DVT0   = 2.8679381     DVT1    = 0.364583
+DVT2   = -0.1457773
+U0     = 457.9817288   UA      = 1.760644E-11
+UB     = 6.60249E-19
+UC     = -2.21616E-11  VSAT    = 2E5         A0      = 0.2569008
+AGS    = 0             B0      = 2.419162E-6 B1      = 2.998423E-6
+KETA   = -0.0151838    A1      = 2.11776E-5  A2      = 0.3164018
+RDSW   = 1.7986E3      PRWG    = 7.186697E-3
+PRWB   = 0.0286192
+WR     = 1             WINT    = 2.280272E-7 LINT    = 4.223411E-8
+XL     = 0             XW      = 0           DWG     = -1.412924E-8
+DWB    = 2.266359E-8   VOFF    = -0.0138159
+NFACTOR = 0.9403671
+CIT    = 0             CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB  = 0             ETA0    = 0.038987
+ETAB   = -4.142228E-3
+DSUB   = 0.2739841     PCLM    = 1.5957826
+PDIBLC1 = -0.7948288
+PDIBLC2 = 2.031474E-3  PDIBLCB = -0.0280342
+DROUT  = 0.5770863
+PSCBE1 = 5.515654E8    PSCBE2  = 3.428003E-5
+PVAG   = 4.075335E-3
+DELTA  = 0.01          RSH     = 85.5        MOBMOD  = 1
+PRT    = 174.3465431   UTE     = -1
+KT1    = -0.3236204
+KT1L   = -7.09202E-10  KT2     = 0
+UA1    = 1.768937E-9
+UB1    = -4.48827E-18  UC1     = -5.6E-11
+AT     = 8.009938E4
+WL     = 0             WLN     = 1           WW      = 0
+WWN    = 1             WWL     = -6.554E-20  LL      = 0
+LLN    = 1             LW      = 0           LWN     = 1
+LWL    = -9.461E-20    CAPMOD  = 2           XPART   = 0.4
+CGDO   = 2.04E-10      CGSO    = 2.04E-10    CGBO    = 1E-9
+CJ     = 4.225482E-4   PB      = 0.9767537   MJ      = 0.438383
+CJSW   = 3.727516E-10  PBSW    = 0.1
+MJSW   = 0.1242771
+CF     = 0             PVTH0   = 0.1503709   PRDSW   = 294.4686286
+PK2    = 0.0257664     WKETA   = 4.349461E-3
+LKETA  = -3.275389E-3
+PVSAT  = 4.053601E4    )
```

Table 1: NMOS device model.

```
* W_min =2.4µm and L_min =0.6µm
* Temperature_parameters=optimized
.MODEL CMOSP PMOS (                     LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 1.39E-8
+XJ     = 1.5E-7        NCH     = 1.7E17      VTH0    = -0.9725622
+K1     = 0.5594978     K2      = 4.242915E-3 K3      = 0
+K3B    = -2.1787058    W0      = 5.024966E-7 NLX     = 1E-9
+DVT0W  = 0             DVT1W   = 0           DVT2W   = 0
+DVT0   = 2.1983824     DVT1    = 0.4590354   DVT2    = -0.0877166
+U0     = 230.1006352   UA      = 3.082914E-9 UB      = 1E-21
+UC     = -8.49253E-11  VSAT    = 1.799169E5  A0      = 0.9968666
+AGS    = 0.1886708     B0      = 1.56806E-6  B1      = 5E-6
+KETA   = -4.636636E-3  A1      = 1.051164E-4 A2      = 0.4948895
+RDSW   = 1.934022E3    PRWG    = 0.0387677   PRWB    = -0.0761681
+WR     = 1             WINT    = 2.519308E-7 LINT    = 3.903552E-8
+XL     = 0             XW      = 0           DWG     = -2.506572E-8
+DWB    = 9.639272E-9   VOFF    = -0.0865101
+NFACTOR = 0.6651504
+CIT    = 0             CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB  = 0             ETA0    = 8.3524E-3   ETAB    = -1.59539E-3
+DSUB   = 0.1864431     PCLM    = 2.4907335   PDIBLC1 = 0.4762146
+PDIBLC2 = 2.561625E-3  PDIBLCB = -0.1        DROUT   = 0.7045912
+PSCBE1 = 1.484087E10   PSCBE2  = 1.453333E-9
+PVAG   = 2.5889735
+DELTA  = 0.01          RSH     = 102.5       MOBMOD  = 1
+PRT    = 22.2970225    UTE     = -1          KT1     = -0.4690262
+KT1L   = 1.73235E-9    KT2     = 0           UA1     = 1.953646E-9
+UB1    = -7.64921E-18  UC1     = -5.6E-11    AT      = -1E5
+WL     = 0             WLN     = 1           WW      = 0
+WWN    = 1             WWL     = -1.205E-20  LL      = 0
+LLN    = 1             LW      = 0           LWN     = 1
+LWL    = 6.268E-21     CAPMOD  = 2           XPART   = 0.4
+CGDO   = 2.24E-10      CGSO    = 2.24E-10    CGBO    = 1E-9
+CJ     = 7.281027E-4   PB      = 0.9583121   MJ      = 0.4969115
+CJSW   = 2.724206E-10  PBSW    = 0.99        MJSW    = 0.3063901
+CF     = 0             PVTH0   = -0.0449356  PRDSW   = 0
+PK2    = -1.037068E-3  WKETA   = -9.521313E-3
+LKETA  = 7.063491E-4   )
```

Table 2: PMOS device model.

Device simulations utilizing these parameters exhibit an excellent fit with the measured *I-V* data for both NMOS and PMOS devices at different bias conditions (see Figures 2-4). The optimized parameters are validated by simulating a benchmark test circuit, a 31-stage ring oscillator included in our process monitor. The ring oscillator consists of a circular string of 31 simple inverters. The layout is custom, not based on standard cells, and is intentionally compact so that the oscillation frequency will be dominated by transistor characteristics. The channels are minimum design rule length, 0.6µm. Device widths are 2.4µm for the NMOS transistor and 4.8µm for the PMOS. The frequency simulation error for low temperature is less than 5% and for high temperature simulation it is less than 10% (see Figure 1). We believe the larger percentage error for high temperature compared to the low temperature is due to the main uses of linear extrapolation in the model to capture the temperature effect (see equations (3), (5), (9), (11) and (12)). Our parameter extraction and optimization are done at room and low temperature points.

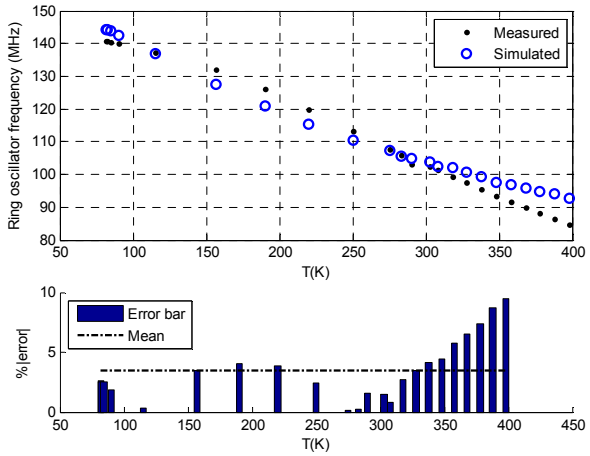

Figure 1: Ring oscillator frequency versus temperature.

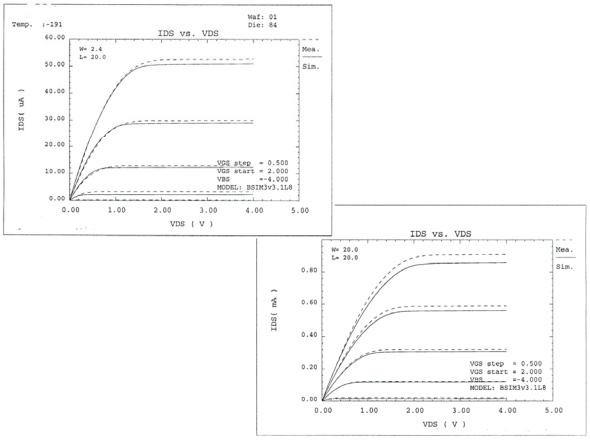

Figure 2: NMOS device channel current versus source/drain voltage at -191^{0}C.

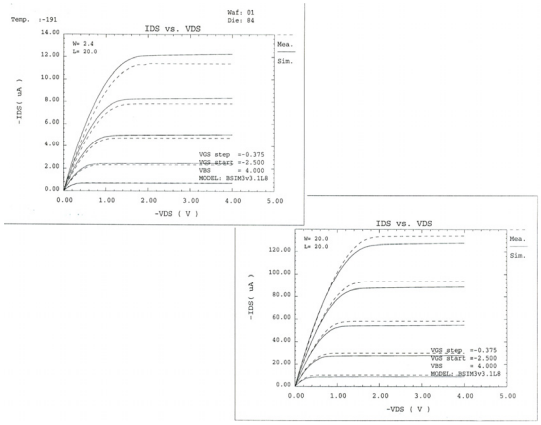

Figure 3: PMOS device channel current versus source/drain voltage at -191^{0}C.

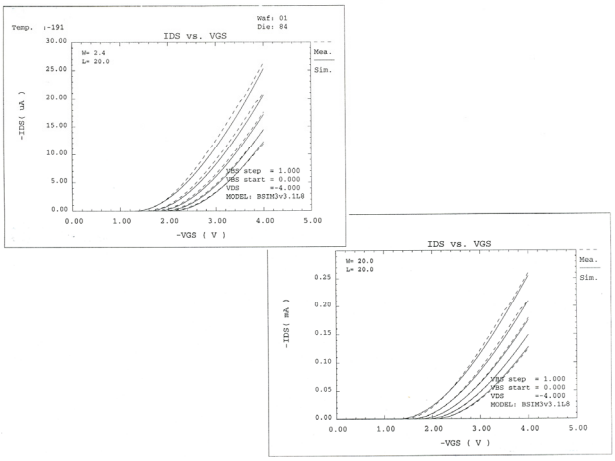

Figure 4: PMOS device channel current versus gate voltage at -191^{0}C.

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