RF Modeling of 45nm Low-Power CMOS Technology

Jing Wang[*], Hongmei Li[**], Li-Hong Pan[*], Usha Gogineni[***], Robert Groves[*], Basanth Jagannathan[*], Myung-Hee Na[*], William Tonti[**] and Richard Wachnik[*]

[*]IBM Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY, 12533, USA, jingwang@us.ibm.com
[**]IBM SRDC, Essex Junction, VT, 05452, USA
[***]Summer Student from Massachusetts Institute of Technology (06/2008 − 08/2008)

ABSTRACT

In this paper, we present an advanced RF modeling work for our state-of-the-art 45nm low-power CMOS technology. Based on carefully designed structures, we extracted a rigorous, hardware-based wiring capacitance model that accurately computes each component of the wirecap network on top of the intrinsic FET. A novel, scalable substrate resistance model was created to well fit relevant hardware data. To obtain accurate on-wafer s-parameter data for the modeling structures at high frequencies (up to 110GHz), we adopted sophisticated deembedding techniques such as Pad-Open-Short and COMPLETE. The results clearly show that our models well match various RF characteristics for devices with a broad range of sizes and measured at different voltage biases. Undoubtedly, these high-quality RF FET models offer circuit designers an indispensable and powerful tool to best utilize our advanced RFCMOS technology.

Keywords: radio-frequency (RF) modeling, RFCMOS, wiring capacitance, substrate resistance, deembedding

1 INTRODUCTION

As the application of CMOS technology in RF circuits becomes more and more popular, accurate modeling of MOSFETs at high frequencies becomes increasingly important [1]. To create high-quality RF FET models, the following requirements should be satisfied:

- Accurate on-wafer s-parameter data are obtained at high frequencies by doing correct deembedding;
- The wiring capacitance (wirecap) network on top of the intrinsic FET is properly modeled;
- A physical and scalable substrate resistance model is included;
- Gate resistance and the Non-Quasi-Static (NQS) effect are accurately fitted for devices at different sizes.

This paper presents an advanced RF modeling work for our 45nm low-power CMOS technology [2]. With a rigorously extracted wirecap network and a set of scalable substrate resistance equations, our RF model well matches accurately-deembedded, high-frequency on-wafer s-parameter data for FETs at a broad range of device sizes (i.e., gate length - *L*, width per finger - *W*, and number of finger - *nf*) and voltage biases. Section 2 reviews the methodology of this work, Section 3 shows the key results for the model-hardware correlation, and Section 4 summarizes the paper.

2 METHODOLODY

2.1 Deembedding

In our previous work [3], we investigated the accuracy of various deembedding techniques published in the literature. And we found that the industry standard 'Open-Short (OS)' technique [4] causes error when *f*>30GHz as compared with the rigorous 4-port COMPLETE deembedding [5], and the 'Pad-Open-Short (POS)' approach [6] greatly improves deembedding accuracy over OS. In this work, therefore, we adopted POS as the deembedding technique for all modeling structures, while COMPLETE is also used for some key device sizes to benchmark the deembedding accuracy.

2.2 Wiring Capacitance (wirecap) Extraction

Figure 1 illustrates the wirecap network to be modeled in our work. To extract the value of each component, we created a series of structures with different layout variants on our test-site (see Table 1). For example, to extract the PC-CA capacitance (*Cpc-ca*), we built a set of devices with the same geometry (*W*/*L*/*nf*) but different numbers of CA per finger. By plotting the gate-to-drain capacitance vs. the number of CA (see Fig. 2), we can obtain *Cpc-ca* (per CA) from the slope of the curve. As summarized in Table 1, all other components of the wirecap network can be extracted using a similar approach. Finally, a set of equations are implemented into our FET model to calculate each wirecap component at different *W*, *L*, *nf* and PC-CA distance.

2.3 Substrate Resistance Model

In our RF model, the BSIM4.5 [7] substrate resistance network is enabled by setting rbodyMod = 1. A scalable equation is built for each substrate resistance component (i.e., RBPS, RBPD, RBPB, RBSB and RBDB) to best fit hardware data for devices at various geometries (*W*/*L*/*nf*).

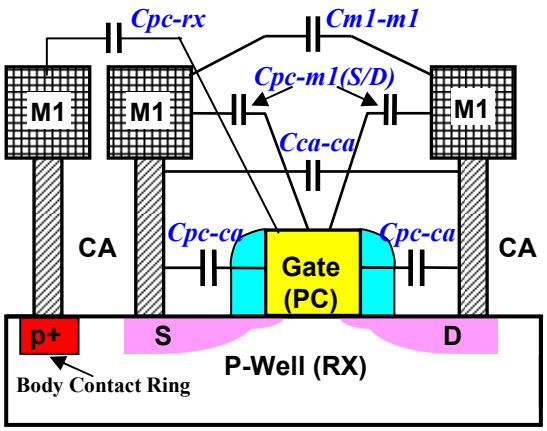

Figure 1: Wirecap network to be modeled.

Wirecap Component	*Structures with different layout variants*	*Extraction Method*
Cpc-ca	fixed *W/L/nf*, various numbers of CA	slope of the *Cgd vs. No. of CA* curve
Cca-ca	same as above	slope of the *Csd vs. No. of CA* curve
Cpc-m1 (S/D)	no CA, no RX, various *W*'s for fixed *L/nf*.	slope of the *Cgs/Cgd vs. W* curve
Cm1-m1	same as above	slope of the *Csd vs. W* curve
Cpc-rx	fixed *W/L/nf* with i) one-sided or ii) two-sided gate contacts	the *Cgs* difference between i) and ii)

Table 1: List of the device structures designed to extract each component of the wirecap network shown in Fig. 1.

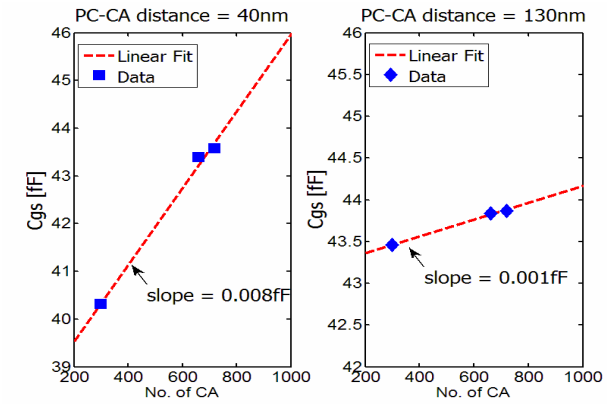

Figure 2: Measured *Cgs* vs. No. of CA curves for 3x0.04x60 (*W/L/nf*) nFETs with two different PC-CA distances, 40nm (left) and 130nm (right). The *Cpc-ca* (per CA) values can be extracted from the slopes of the two dashed lines as 0.008fF and 0.001fF, respectively.

2.4 NQS fitting

BSIM4.5 provides two model parameters, XRCRG1 and XRCRG2, for NQS fitting. In this work, we built geometry-dependent equations for both parameters in our model to obtain a good match with hardware data over a large range of device sizes.

3 RESULTS

This section reviews the model-hardware correlation for various RF characteristics of the modeled FETs. In our work, the on-wafer s-parameter data for devices at different geometries (*W/L/nf*) were collected at up to 110GHz with a 2-port, common-source configuration. As mentioned in Section 2.1, the raw measurement data were carefully deembedded by using a POS technique to obtain the accurate intrinsic device characteristics for model parameter extraction.

Figure 3 compares the simulated gate input capacitance vs. hardware data (symbols) for a 1.5x0.04x20 nFET, with (solid lines) and without (dash lines) the wirecap model enabled. Clearly, the wirecap components account for a significant portion of the total gate capacitance, e.g., >15% at the ON-state and ~30% at the OFF-state. For this reason, an accurate description of the wirecap network is essential for building high-quality RF FET models.

Figure 4 shows the measured (symbols) and simulated (lines) substrate resistance (R_{sub}) data for devices at different geometries. The R_{sub} values are extracted from the relevant s-parameter data by adopting Eq. (29) in Ref. [1]. It is clear that our scalable equations correctly describe the R_{sub} dependence on *W*, *L* and *nf* of the modeled FETs.

In Fig. 5, we demonstrate the gate input resistance (R_{gate}) fitting for three different nFETs. As expected, the 5x0.04x20 nFET displays the largest R_{gate} among all the three devices due to its largest *W* and smallest *L*, for the gate polysilicon resistance is proportional to *W/L*. While the 1.5x0.5x20 nFET achieves a higher R_{gate} than the 1.5x0.2x20 device because the *L*=0.5µm device suffers strong NQS effect, which, as shown in Fig. 6, has been correctly modeled in our work.

Figures 7-8 show the measured (symbols) and simulated (lines) power gains (MAG/MSG) and RF current gain for nFETs at different geometries and voltage biases. It is clear that the model results well match the hardware data for these critical RF performance metrics at the full frequency range of measurement. Finally, Fig. 9 illustrates the cut-off frequency vs. the gate bias for both (a) nFETs and (b) pFETs at three different gate lengths (40nm, 100nm and 260nm). It can be concluded from the results that our model accurately calculates the RF performance for both n-type and p-type FETs at the full dynamic voltage range (0V – 1.1V) for devices at various geometries. Therefore, these high-quality RF FET models provide circuit designers a powerful tool to search for the optimum device geometry and voltage bias conditions for their circuit applications.

NSTI-Nanotech 2009, www.nsti.org, ISBN 978-1-4398-1784-1 Vol. 3, 2009

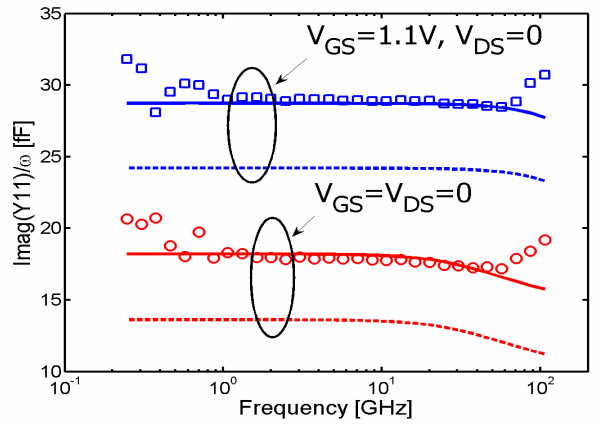

Figure 3: Gate input capacitance, *Imag(Y11)/ω*, vs. *Freq.* curves for a 1.5x0.04x20 (*W/L/nf*) nFET. The symbols are for hardware data, and the solid (dash) lines are for the simulation results with (without) the wirecap model enabled.

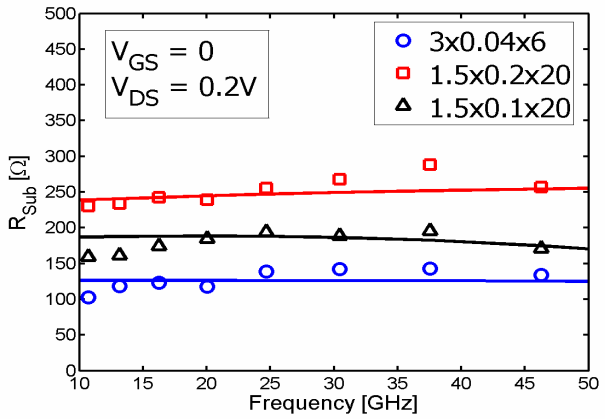

Figure 4: Extracted R_{sub} vs. *Freq.* curves for nFETs at three different sizes (*W/L/nf*). The symbols are for hardware data and the solid lines for the model results.

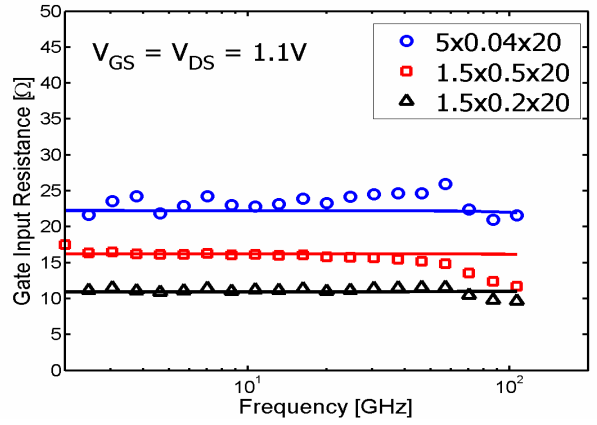

Figure 5: Measured (symbols) and simulated (solid lines) effective gate input resistance, *Re{(1+S11)/(1-S11)}·50Ω*, vs. *Freq.* for nFETs at three different geometries (*W/L/nf*).

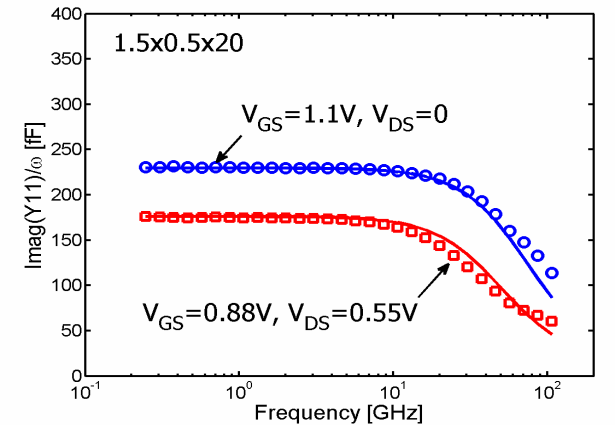

Figure 6: Measured (symbols) and simulated (solid lines) gate input capacitance, *Imag(Y11)/ω*, vs. *Freq.* for a *L*=0.5µm nFET under two biases. The non-quasi-static (NQS) effect is observed and properly modeled.

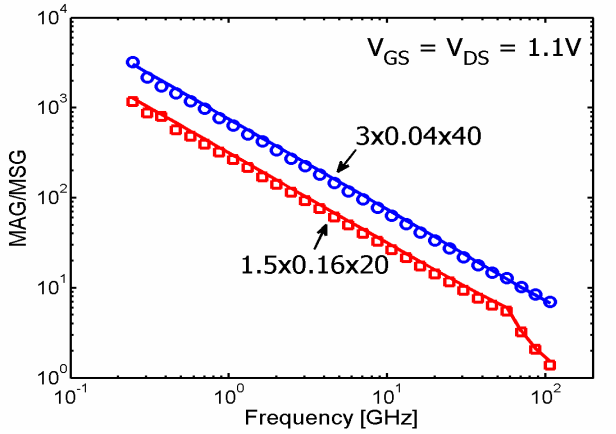

Figure 7: Maximum Available Gain (MAG) or Maximum Stable Gain (MSG) vs. *Freq.* for nFETs at two different sizes (*W/L/nf*). The symbols are for hardware data and the solid lines for the model results.

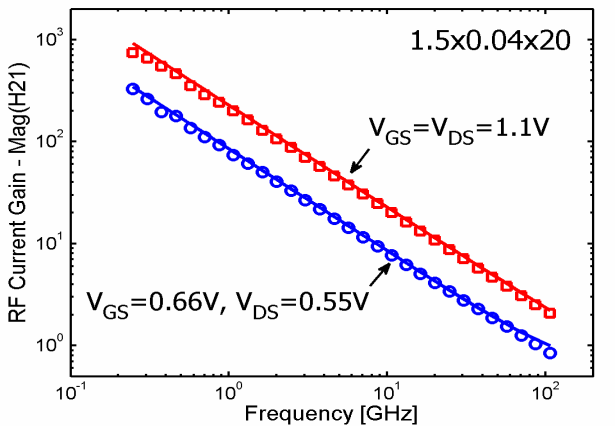

Figure 8: RF current gain, *Mag(H21)*, vs. *Freq.* curves for a 1.5x0.04x20 (*W/L/nf*) nFET. The symbols are for hardware data and the solid lines for the model results.

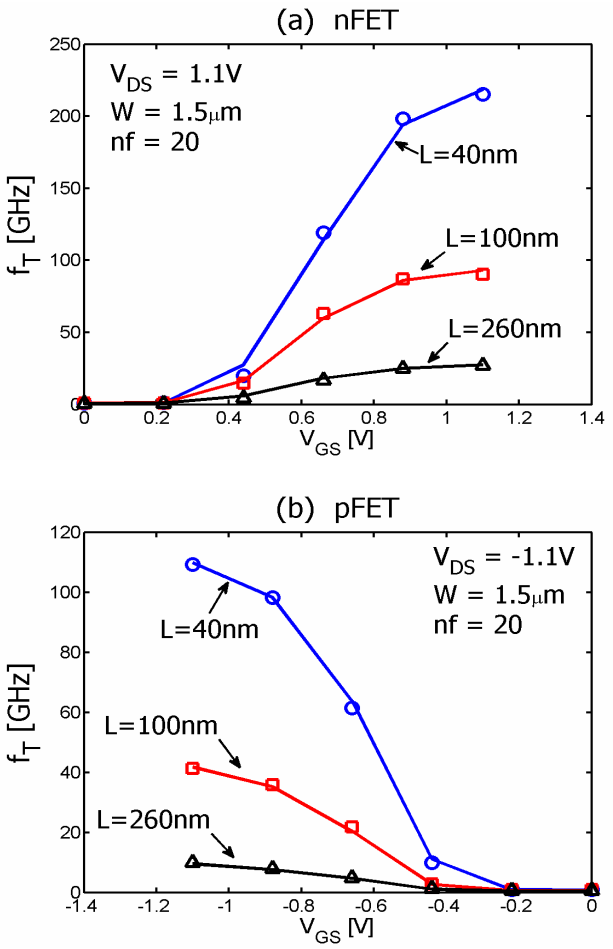

Figure 9: Cut-off frequency (f_T) vs. V_{GS} curves for (a) nFETs and (b) pFETs, each at three different gate lengths (L = 40nm, 100nm, and 260nm). W=1.5μm, nf=20 and $|V_{DS}|$=1.1V. It is clear that the model results (solid lines) well match the measurement data (symbols) at a broad range of device geometries and voltage biases.

4 SUMMARY

To accurately model 45nm bulk MOSFETs for RF circuit design, we created a rigorous, hardware-based wiring capacitance model and a novel, scalable substrate resistance model. The simulation results with our RF FET models display a good agreement with high-frequency measurement data carefully deembedded by using advanced techniques (e.g., Pad-Open-Short or 4-port COMPLETE), for a large range of device sizes and voltage biases. Without a doubt, our high-quality RF FET models are critical for the enablement of this 45nm RFCMOS technology, and the methodology developed in this study is also valuable for creating RF models for future technology nodes.

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