Dynamic Charge Sharing modeling for surface potential based models

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ABSTRACT

Adaptative body bias has been recently pointed out to boost device performance and to reduce power consumption. An accurate description of back bias dependence is required to correctly model the electrical behaviour of such devices. This paper is focused on the electrical characterization and the surface potential based compact modeling of the threshold voltages shifts induced by back bias polarization for various gate length at various drain voltages. The description of the "dynamic charge sharing" model is proposed and compared to the "charge sharing" model originally developed for threshold voltage models. Electrical data from the 45 and the 65 nm nodes have been characterized to underline the threshold voltages shifts versus back bias polarization behavior from long to short channel. Finally the electrical model behaviour for back bias polarization has been compared to the experimental data.

Keywords: surface potential based models, MOSFET, dynamic charge sharing, short channel effects, body effect.

INTRODUCTION

Technology tuning by design means have been recently pointed out. Particularly, the possibility of back bias polarization ($V_B$) to tune the threshold voltage ($V_T$) has been commonly adopted in advanced devices [1]. As a consequence the core of the compact models require an accurate description of the $V_T$ shift due to $V_B$ under low and high drain voltages ($V_D$) but also an accurate subthreshold slope and drain induced barrier lowering (DIBL) modeling.

The dependence of the threshold voltage versus back bias is commonly referred as the body effect. It is well known that the uniformly doped long channel exhibits a linear dependence of the $V_T$ shift as a function of $\sqrt{2\Phi_f + V_B - \sqrt{2\Phi_f}}$ [2], where $\Phi_f$ denotes the Fermi level. This is no longer true in shorter devices as demonstrated in literature and in this work for two advanced technological nodes, namely the 65 and the 45 nm. Among the short channel effect (SCE) commonly addressed by electrical characterization, one can note the DIBL and the change in the subthreshold slope.

The Wu’s charge sharing model [3] is based on the modulation of the depleted charges through a geometrical sharing coefficient, and has shown a good agreement with experimental data. However this description has been developed only for $V_T$ based models and is no longer sufficient for surface potential based models. In the next section, an original surface potential based model is proposed. Then the electrical behaviour of this model under $V_B$ polarization is compared to experimental data.

DYNAMIC CHARGE SHARING

MODEL DESCRIPTION

The electric field distribution under the gate is modified due to the presence of the drain and source junctions. This effect becomes dominant as the channel length becomes smaller and the substrate back bias polarization becomes larger. Fig.1 shows the source and drain depletion width both calculated with two dimensional analysis (TCAD), see in Fig.1a and a schematic view in Fig.1b.

The "charge sharing" approach is derived from a reduction of the depletion charge controlled by the gate by a geometrical factor, which depends on the variation of $X_s$ and $X_D$ representing source and drain depletion width. Fig.2a represents a schematic view of this "charge sharing" approach proposed by Wu’s model where:

$$X_{s,d} = \sqrt{\frac{2\varepsilon_{SI}}{qN_{pocket}}} (V_{bi} + V_{(S,D)B}), \quad (1)$$

with $V_{bi}$ denoting the source and drain built in potential, $N_{pocket}$ the doping level of pockets.
We propose to refine the Wu’s model using a “dynamical charge sharing model”, where dynamic refers to the evolution of the geometrical sharing coefficient with surface potential $\Psi_S$ (gate voltage $V_G$, $V_B$, and $V_D$) through the parameter $x_s$ and $x_d$ described in Fig. 2b:

$$x_{s,d} = \sqrt{\frac{2\epsilon_{SI}}{qN_{pocket}} (V_{fb} + V_{S,D}) B - \Psi_S}, \quad (2)$$

The effective depleted charge can be rewritten as a function of the long channel depleted charge:

$$Q_{(short)} = Q_{(long)} * F(\Psi_S), \quad (3)$$

where $F(\Psi_S)$ is the geometrical sharing coefficient extracted from the trapezoidal shape of the effective charges (Fig. 2):

$$F(\Psi_S) = 1 - \frac{x_s + x_d + X_s + X_d}{2L_{gate}} \quad (4)$$

The $\Psi_S$ dependence of the geometrical sharing coefficient is shown in Fig.3 for various $V_B$ (0, -0.22, -0.44, -0.66, -0.88, and -1.1 Volts). The dynamic description exhibits a square root evolution (due to the presence of $x_{s,d}$ (4)) in the trapezoidal description, and a constant shape (obtained using the hyp smoothing function) over the threshold voltage at $2\phi_f + VB$.

In order to extend this concept to surface potential based models, this new geometrical coefficient $F(\Psi_S)$ is applied on the fixed charge component of the original implicit surface potential equation (SPE) [4]:

$$(V_{gb} - V_{fb} - \Psi_S)^2 = \gamma^2 \Phi_T e^{\frac{\Psi_S}{\Phi_T}} + \gamma^2 \Psi_S^2 F(\Psi_S)^2 - \gamma^2 \Phi_T^2 + \gamma^2 \Psi_S e^{\frac{2x_s + x_d}{\Phi_T}} \left(e^{\frac{\Psi_S}{\Phi_T} - \frac{\Psi_S}{\Phi_T}} - 1\right), \quad (5)$$

where $\Phi_T$ is the difference between electron and holes quasi-fermi levels, $\Phi_T$ the thermal voltage, $\Phi_f$ the Fermi level, and $V_{fb}$ is the flat-band voltage. The second term in the r.h.s. of (5) can be identified as the square of the effective depletion charge ($q_{dep}$) modified by the dynamical sharing coefficient:

$$q_{dep} = \gamma \sqrt{\Psi_S} * F(\Psi_S) \quad (6)$$

The modification of the SPE is affecting the electrostatic behaviour of the MOSFET, that leads to $\Psi_S(V_G)$ evolution. The sharing of the depleted charges because of source and drain junctions is now intrinsically implemented in the electrostatic resolution of the SPE through the $F(\Psi_S)$ coefficient. The new SPE is solved iteratively with Newton’s method convergence. Fig.4 (respectively Fig.5) shows the resulting $\Psi_S(V_G)$ dependence for long (respectively short) devices resulting from the “dynamic charge sharing” model.

**Figure 3:** Geometric Charge Sharing - Constant and Dynamic sharing coefficient evolution as a function of $\Psi_S$ - $L_{gate} = 100nm$, $N_{pocket} = 1e17at/cm^3$, $N_A = 7e17at/cm^3$, $T_{ox} = 1.8nm$, $N_{junction} = 1e20at/cm^3$.

**Figure 4:** Surface potential from dynamic charge sharing model ($V_B=0$,-0.22,-0.44,-0.66,-0.88, and -1.1 Volts) - $L_{Gate} = 10 \mu m$ - geometric charge sharing coefficient negligible.

**Figure 5:** Surface potential from dynamic charge sharing model ($V_B=0$,-0.22,-0.44,-0.66,-0.88, and -1.1 Volts) - $L_{Gate} = 80nm$. Short devices exhibit a smaller $V_B$ dependency than the long ones. Indeed for the smallest devices, the relative amount of depleted charges shared between S/D and the gate becomes larger. A general equation for the subthreshold slope comes from the direct derivation of the drain current expression [5]:
The drain current calculation is calculated from the Brew’s charge sheet model [6], where the inversion charge is expressed under the charge sheet approximation. Derivating the dynamic charge sharing equation from the Brews’ approach leads to the inversion charges ($q_i$) required for the drain current calculation:

$$q_i(\Psi_S) = (V_g - V_{fb} - \Psi_S) - \gamma \sqrt{\Psi_S} F(\Psi_S)$$  (8)

The drain current ($I_D$) is derived from the drift-diffusion approach as follows:

$$I_D = \int_{Q_{in}}^{Q_{out}} \mu_n q_i(\Psi_S) d\Psi_S + \int_{Q_{in}}^{Q_{out}} \mu_n dq_i$$  (9)

### EXPERIMENTAL DATA AND MODEL VALIDATION

Experimental Id-Vg data from the 45 nm node for long channel device (Fig.7, Lgate=10 μm) and for short channel device (Fig.8, Lgate=45 nm) are presented for various $V_B$ (0, -0.22, -0.44, -0.66, -0.88, and -1.1 Volts) and for two $V_D$ values ($V_{dd}=0.05$ Volts and $V_{dd}=1.1$ Volts). Simulated Id-Vg curves based on our dynamic charge sharing model have been superimposed on experimental data (Fig.7 and Fig.8)

Fig.7 shows that the Id-Vg at various $V_B$ for high $V_D$ quasi perfectly overlaps the Id-Vg at various $V_B$ for low $V_D$. For short devices, see Fig.8, Id-Vg at various $V_B$ for high $V_D$ is shifted from the Id-Vg at various $V_B$ for low $V_D$ (SCE and DIBL). Moreover, one can notice that the Id-Vg at various $V_B$ is wider for longer devices, whereas for short devices, the Id-Vg at various $V_B$ is shrinking for high $V_B$ values especially for high $V_D$.

In order to give a quantitative description of this phenomenon, the threshold shifts due to $V_B$ are extracted using an original method described in [7]. Results are presented in Fig.9, Fig.10, Fig.11 for various Lgate.

The dotted lines refer to an effective constant doping extracted at $V_B=0$. One can notice that this method traduces the deviation to a “long” channel behaviour. This extraction method enables a good visualization to compare the channel length reduction impact on the $V_T$ controlling the $V_T$ shifts. We can notice that even though

$$S = \frac{kT}{q} \ln(10) \left( \frac{dV_G}{d\Psi_S} \right)$$  (7)

Fig. 6 shows that for shorter devices the shape of the $d\Psi_S/dV_G$ curve is modified and the subthreshold slope is intrinsically modified through $\Psi_S$ variations.
the experimental data belong to two different technological nodes, their behaviour is particularly similar.

For long channel devices, the $V_T(V_D)$ relation exhibits almost a constant shape, see Fig.9. The impact of source and drain junction is negligible. The small deviation only occurs due to non uniform vertical doping [7].

The $V_T(V_B)$ relation exhibits a significant deviation to the long channel devices for short devices, see Fig.10 and Fig.11. The impact of source and drain junction becomes non negligible. And the depleted charges initially controlled by the gate for the “long” device are shared, for short devices, with source and drain junctions. The deviation becomes larger for smaller Lgate and. Moreover, there is a splitting effect due to $V_D$ polarization that appears traducing the DIBL. The deviation to the dotted line is increasing for high $V_D$.

For the shortest devices, see Fig.11, the charge sharing of the depleted charges leads to almost a zero $V_T$ shift under $V_B$ polarization.

It is observed that this effect is enhanced with the reduction of Lgate and amplified with high $V_D$ values, which is well reproduced by our model.

CONCLUSION

This paper refers to the electrical characterization of the $V_T(V_D)$ for two advanced technological nodes, namely 65 and 45nm, that confirms a lost of control for tuning the $V_T$ as a function of $V_D$ polarization for the shortest devices. This sharing effect is enhanced for high $V_D$ polarization. For design applications, the surface potential based models should take into account this $V_T(V_D)$ behaviour.

A "dynamic charge sharing model" has been proposed to take into account these effects in surface potential based compact models. This model relies on the $\Psi_s$ dependence of the geometrical sharing coefficient injected in the surface potential equation. The range of applications of this model has been proved for gate length from nominal to 10 $\mu$m devices, $V_D$ up to $V_DD$, and $V_B$ from 0 to -1.1 Volts. This modeling approach enables to reproduce the electrostatic behaviour observed in experimental data (SCE, DIBL, subthreshold slope variations and $V_T(V_B)$ dependency), because it intrinsically modifies the $\Psi_s(V_D)$ evolution. This model also modifies the terminal charges, and thus the capacitive response of the device. This model has also been successfully applied to non-volatile memory [8].

REFERENCES