PSP Model Equations Extension for Statistical Estimation of Leakage Current in Nanometer CMOS Technologies Considering Process Variations

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ABSTRACT

A novel analytical extension to the PSP transistor model is proposed for static leakage estimation of CMOS circuits considering statistical process variations. Probability equations are inserted directly into the PSP transistor model. Since those equations are completely generic, the proposed methodology is straightforwardly applicable to any technology node. The extended PSP model has been tested and compared to extensive Monte-Carlo simulations of CMOS circuit blocks having transistor's gate length of 45nm (STMicroelectronics technology). The results show that the methodology is accurate in estimating the shape of the probability distribution and the mean value of the leakage current (error smaller than 2%), reducing at least by a factor of a hundred the computational effort required for a Monte-Carlo analysis.

Keywords: leakage, Monte-Carlo, PSP

1 INTRODUCTION

Circuit variability refers to deviations of device parameters (e.g., gate length, supply voltage, oxide thickness, etc.) from nominal values. To achieve a high product yield, designers add design margins to both power and speed performance in order to accommodate the worst design spread. In that condition the design is often pessimistic leading to a large power penalty to meet the performance goals under the worst case conditions. Nowadays, the standard digital design flow does not take into account the statistical variability of the leakage power consumption, and only post-characterization tuning techniques have been developed to tighten the distribution of maximum operating frequency and maximum power consumption [1].

Although Monte-Carlo analyses could mitigate this problem by accurate estimations of circuit leakage considering process variations, they have long simulation times, and, hence increase the design cycle. Therefore, an efficient analytical statistical estimation and modeling methodology of the total leakage current, considering the effects of process parameter variations, is needed for designing CMOS circuits in advanced technologies [2].

In the past years, a number of works have focused on the problem of accurate prediction of leakage in digital

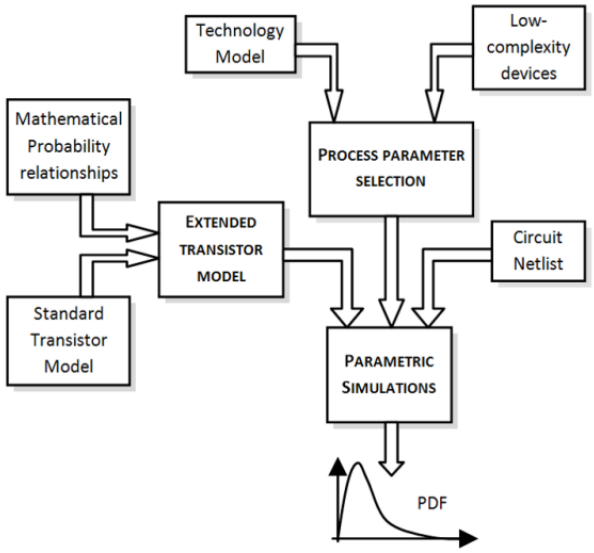

Fig. 1 - Main steps of the proposed analytic leakage estimation methodology

circuits in the presence of variations. The previously proposed statistical leakage analyses approaches can be classified in two main groups. The first set of techniques approximate the transistor leakage currents with empirical equations (whose parameter are found by curve-fitting) or use Taylor expansion series to approximate the logarithmic expression of the leakage current [3-4]. The second set of methodologies proposes transistor models (developed simplifying the PSP/BSIM models, or elaborating manufacturing data) aware of process variations [5]. The main drawback of the first group of statistical techniques is that their reliability with respect to manufacturing strongly depends on the correctness of the empiric relations used for the leakage current. This is particularly true in recent technology nodes due to the extremely complex impact of process variations on leakage currents. About the second group of methodologies, the major disadvantage is that the set of proposed equations needs new coefficients that have to be pre-determined (by fitting SPICE simulations or device extraction data for each library's cell). This time consuming pre-elaboration phase is often under-estimated in the overall computational cost count. Furthermore IC manufacturers already have their characterized standard cell libraries and would like to avoid new characterizations before applying statistical leakage analysis.

The goal of the proposed PSP model extension is to obtain a time-efficient and accurate estimation of the PDF of the leakage current of a complete digital circuit.

Using this approach, time consuming Monte-Carlo based simulations on high-complexity circuits can be avoided. It can be easily applied to estimate the leakage probability distribution considering one, two, or more process parameters varying simultaneously.

Fig. 1 describes the three main phases of the current methodology implementation:

- Probability analytical relationships are included in standard PSP transistor models
- Monte Carlo simulations are performed on simple devices (single transistor or small logic gates): the process parameters whose variations impact the leakage spread are identified. This step is performed only once for each technology node. Since the simulations are performed on low-complexity devices, the computational time is extremely short.
- Parametric simulations are performed, using the extended set of PSPS equations on the real circuit sweeping, with a discrete step, the variation range of the identified process parameters. Accuracy of the result and computation time can be selected setting the right number of parametric simulations.

2 DOMINANT PARAMITER SELECTION

Previous works report that each leakage contribution in a CMOS circuit depends on more than one process parameter and has different sensitivity with respect to those parameters variation [6]. Moreover, extensive Monte-Carlo simulations have shown that the impact of process parameters variations on the leakage probability distribution is different for each technology node.

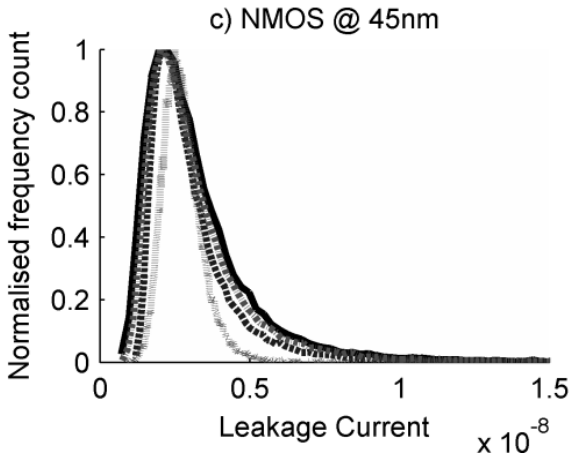

Fig. 2 - Monte-Carlo simulations. Impact of gate length and channel doping on the leakage current distribution of an NMOS transistor in 45 nm technology node

In particular, 45nm technology node is subject to a number of variation effects that are well documented in the literature [7]. Hence, a key step in the proposed methodology is the selection of the process parameters whose variation impacting the leakage PDF. Several approaches have been proposed in the past (e.g. Design of Experiment, Principal Component Analysis) to identify the most relevant process parameter for a specific technology node.

In this work a simple approach based on Monte Carlo simulation have been chosen, although any of the previous approach could be used. Fig. 2 shows Monte-Carlo simulations highlighting the impact of some process parameters on the probability distribution of the total leakage current for a 45nm gate length NMOS transistor. The PDFs, taking into account variations in all the process parameters, look like lognormal-shaped curves. In 45nm, to have a good estimation of the leakage probability distribution considering all the process parameters, it is necessary to simulate simultaneous fluctuations of the gate length and of the channel doping level.

3 PSP MODEL EXTENSION

Classically, to estimate the PDF of the leakage current as a function of a process parameter, a great number of Monte-Carlo simulations are performed using the approach: a single value of the process parameter is extracted randomly from the sampling space, the circuit is simulated, and the out-coming leakage value is used with a binning methodology to construct the PDF curve.

The proposed general framework can be easily used to model the total leakage current with respect to different process parameters variations (Lgate, Tox, Vth0, …) of a single transistor or a complex logic circuit, without using MC simulations.

For clarity of purpose, in the following equations, the methodology is illustrated analyzing the variability of the leakage current with respect to a process parameter, the drawn channel length.

Given the PDF of the gate length, $L = f_x(L)$, the mathematical dependence between the leakage current, I, and L, $I = h(L)$, and its inverse function $L = h^{-1} = g(I)$, the PDF of I can be expressed using Eq. 1 [8]:

$$PDF(I) = f_y(I) = \frac{f_x(g(I))}{h'(L)} \quad (1)$$

where $h'(L)$ is the first derivative of the function $h(L)$.

To compute the PDF of the leakage current, it is essential that: (1) the function g is a closed-form expression and (2) the function h is differentiable over the given range of currents [3]. Unfortunately, the complexity of the relationship between leakage current and channel length does not allow the derivation of $g(I)$ to satisfy those two conditions.

The approach proposed in this paper is different: the PDF of the total leakage current can be expressed directly

as a function of L, i.e. $PDF(I_{(L)})$, by exploiting the intrinsic calculation capabilities of the electrical simulators and the PSP model equations. Hence, the function $L = g(I)$ is not used any more.

From a mathematical point of view, assuming that the drawn gate length has a Gaussian distribution (but this could be any probability distribution) with a fixed mean, μ_L, and standard deviation, σ_L, the *PDF(I)* can be written as in Eq. (2):

$$PDF(I) = f_y(I) = \frac{1}{h'(L)} \cdot f_x(L)$$
$$f_y(I) = \left(\frac{1}{h'(L)}\right) \cdot \left(\frac{1}{\sigma_L\sqrt{2\pi}}\right) \cdot exp\left(\frac{-(L-\mu_L)^2}{2\sigma_L^2}\right) \quad (2)$$

Where $f_x(L)$ represents the PDF of the gate length and is pre-determined by the technology model (usually a normal distribution); $h'(L)$ represents the first derivative of the leakage current respect to the process parameter.

At different levels of hierarchy of a CMOS circuit the determination of the function $h'(L)$ is easy and straightforward. At transistor level the total leakage can be modeled as a sum of independent voltage controlled current sources [9], where each source describes one leakage contribution I_{sub}, I_{gate}, I_{BTBT}, and I_{GIDL}. Using the same idea, at gate level or at circuit level, the total leakage can be estimated adding the currents going through all the logic gate terminals connected to the supply rail. Consequently, the first derivative of the total leakage current as function of the gate length, $h'(L)$, can be always calculated as a sum of independent partial derivatives.

This way, any approximated relation between the leakage components and the gate length is avoided since $f_x(L)$ and $h'(L)$ can be directly enclosed into PSP code.

As already mentioned, in 45nm technology node, the biggest impact on the spread of the leakage current is determined by the variations of the gate length and the fluctuation of the channel dopant concentration. Hence, these two process parameters are considered to estimate the PDF of the leakage current with the proposed methodology.

In this work, the PSP model (coded in Verilog-A) is integrated by four functions: $h'(L)$, the analytic first derivative of the leakage currents with respect to the gate length; $f_x(L)$, the probability density function of the gate length; $m'(ChDop)$, the analytic first derivative of the leakage currents with respect to the dopant concentration; $d_x(ChDop)$ the probability density function of the dopant concentration.

Combining (as in eq. 2) the four previous equations, two PDF of the leakage current are obtained: one function of the gate length and one function of the channel doping concentration (general for acceptors or donor atoms).

From a coding point of view, the current derivates are expressed with respect to the two PSP parameters **LVARO** and **NSUB**, representing the variation in the effective gate length and the variation in the number of doping atoms, respectively. Due to the complexity of the PSP model and to the structure of the Verilog-A code, the derivation of the leakage currents equations is performed backwardly: starting from the final expressions of the leakage current and moving upward into the code up to the expression of the single two process parameters (passing through all the specific macro functions where needed).

The resulting extended model remains completely generic for NMOS and PMOS transistors thanks to the PSP parameter **TYPE** (which assume the value '+1' for N channel and '-1'for P channel).

Several test simulations have been performed to fully verify the correctness of the inserted equations, comparing graphically the analytic derivative results with numeric derivations.

4 EXPERIMENTAL RESULTS

The extended transistor model is successively used in an electric simulator (ELDO) to perform parametric simulations.

Considering three leakage-influent process parameters (transistor gate length, acceptors atoms doping concentration and donor atoms concentration) it is necessary to make a multiple parametric electrical simulation in which the three parameters are swept from their theoretical minimum value $(\mu - 3\sigma)$ to their theoretical maximum $(\mu + 3\sigma)$. In the same time, other SPICE parameters are fixed using standard technology model cards. The result of the simulation is a series of probability distribution curves (mainly lognormal-shaped). Each curve represents the PDF of I, function of one parameter, and is parameterized by the other two process parameters. To obtain the final *PDF(I)* all the curves are recursively summed together, using as a weighting function the PDF of the other parameters. To calculate the mean and standard deviation (SD) of the total leakage current distribution, a numerical integration of $f_y(I)$ is performed over the given range of leakage currents.

A comparison between the *PDF(I)* obtained with the proposed methodology and an extensive Monte-Carlo simulation of a simple logic gate circuit (a two input NAND gate followed by a two input OR gate) is shown in Fig. 3. The plots of the PDF's, including the tail portion, fit well and have a lognormal shape.

The proposed methodology has been applied to some ISCAS [10] test circuits, the input vector being chosen randomly. The total leakage current of each gate highly depends on the input vector assignment. Table 1 compares the PSPS extended model results to Monte-Carlo simulations for the ISCAS circuits synthesized with 45nm STMicroelectronics Low Power technology. The drawn gate length, the NMOS channel doping and the PMOS channel doping are assumed to be normally distributed with independent ±3σ variation around their respective median point. The table shows that the error in estimating the mean leakage current with the proposed methodology, compared

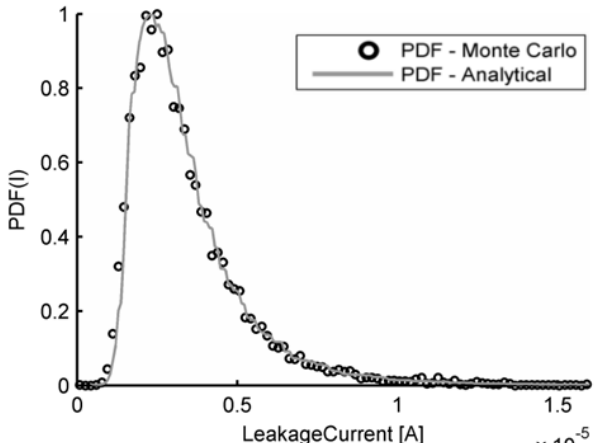

Fig. 3 - Comparison of the Monte-Carlo PDF and the PDF resulting from the extended PSP model

with extensive Monte-Carlo simulations, is typically around 1.5%.

The error in estimating the standard deviation is lower than 6%. The spread in the SD estimation error values is due to the shape of the leakage probability distribution: the error is smaller for a lognormal shaped distribution and larger in the case of a normal distribution.

Moreover, it is important to notice that, to obtain the analytical results, about one thousand simulations have been used, whereas with the Monte-Carlo approach, fifty thousand simulations have been performed. The difference in computation time between a simulation with the standard PSP model and a simulation with the PSP model plus the probability equations can be considered extremely small due to the light impact those equations have on the overall length of the model code.

5 CONCLUSIONS

We have presented, in this paper, a novel PSP extension to estimate distributions of the leakage current of CMOS circuits in presence of process statistical variations. Fluctuations of several process parameters can be considered simultaneously. During the analysis, all the main leakage currents are considered and the complete PSP equation set is used without any approximation. The proposed approach is not limited to the leakage estimation of a single transistor but also extended to gate-level and circuit-level analysis. The proposed model extension has been verified by means of extensive Monte-Carlo simulations of circuit blocks having 45nm transistor gate length. The results show that the approach is extremely accurate in estimating the overall mean and standard deviation of the total leakage current while saving on the computational effort required for a Monte-Carlo analysis.

TABLE I
COMPARISON BETWEEN MEAN VALUES AND SDS OF SOME ISCAS CIRCUIT, OBTAINED WITH MONTE-CARLO (MC) SIMULATION AND WITH THE PROPOSED (PSPE) PSP EXTENSION

Circuit	Mu (MC)	Mu (PSPE)	E%	SD (MC)	SD (PSPE)	E%
C432	3,4e-06	3,5e-06	2,7	2,0e-06	2,0e-06	0,6
C499	5,3e-06	5,5e-06	3,1	3,0e-06	3,0e-06	1,1
C1908	7,0e-04	7,1e-04	0,6	8,6e-05	7,8e-05	9,8
C2670	1,2e-04	1,2e-04	1,1	1,7e-05	1,6e-05	5,6
C3540	3,9e-04	3,9e-04	0,7	5,0e-05	4,6e-05	7,8
C5315	1,2e-03	1,2e-03	0,6	1,5e-04	1,4e-04	7,8
C6288	4,4e-05	4,5e-05	2,5	2,7e-05	2,5e-05	4,8
C7552	6,9e-04	6,9e-04	0,9	8,9e-05	8,2e-05	8,2
Average			**1.5**			**5.7**

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