A Physical Based Hot Carrier Injection Compact Model for Nanoscale FinFET

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ABSTRACT

A detail analysis for nanoscale FinFET performance degradation induced by the Hot Carrier Injection (HCI) is given in this paper, and a physical based HCI compact model adapted to all the operation modes is presented. It is concluded that in the depletion and weak reverse region, the degradation of carrier mobility is the dominant impact on the current decrease; in the strong inversion region, the current decrease is determined by the loss of inversion charges trapped in the interface states. With the analysis, a compact HCI model for Nanoscale FinFET is derived and validated in both forward and reverse operation mode. The simulation result agrees very well with the measured data.

Keywords: Reliability, HCI, model, mobility, Nanoscale FinFET.

1  INTRODUCTION

The nanoscale FinFET has been believed the most promise candidate to take over the traditional Bulk MOSFET due to its excellent scaling characteristics and high integrated density. With the aggressive scaling down of the device dimension, however, Hot Carrier Injection (HCI) has become one of the most important issues for next generation highly integrated circuit due to large electrical field [1-7]. Although many reports have been carried out for interface states analysis [8-12] and the impact on the current-voltage characteristics [13][14], a compact model is necessary to take over the partial model and suit for the SPICE simulation of FinFET based circuits.

With the effect of hot carrier injection, the performance decrease is supposed to be induced by the loss of the inversion charges and the carrier mobility degradation induced by the interface states. In the previous theory [13-16], the degradation of mobility is only relative to the interface states density, but this assumption does not match well with the experimental results as shown later in our work. As a result of the asymmetric distribution of the interface states caused by HCI, the drain current degradation, especially in the saturation region, shows a great distinction between forward and reversed (source and drain exchanged) operation mode.

The content of this paper is organized as follows: a physical based HCI compact model for Nanoscale FinFET is derived in section 2; the simulation results and detail analysis of the impact of HCI to the current characteristic in different operation mode are shown in section 3; finally, a conclusion is given in section 4.

2  COMPACT HCI MODEL DEVELOPMENT

The schematic of the fabricated Nanoscale FinFETs and its cross section after HCI stress are shown in Fig. 1(a) and (b). $t_{si}$, $N_i$ and $l$ are defined as the Si body thickness, interface state density and the damage region length, respectively.

Due to the high gate-drain electrical field, the interface states caused by HCI mainly distribute near the drain region. The interface states are supposed to be acceptors and the density distributed along the channel is $N_i(y)$.

The inversion charge will decrease for the captive by the acceptors. Therefore the inversion charge can be expressed by

$$Q_i(y) = -C_{ox}\left[V_{gb} - V_{th} - V(y)\right] + qN_i(y)$$

Fig.1 (a) Schematic view of bulk Nanoscale FinFET, (b) The cross section of Nanoscale FinFET suffered from HCI.
Where \( Q_n(y) \) is the inversion charge concentration; \( C_{ox} \) is the gate oxide capacitance; \( V_{gb}, V_{ddo} \) and \( V(y) \) present the gate voltage, threshold voltage and surface potential respectively; and \( q \) is the magnitude of electron charge. The drain current is obtained from the inversion charge as

\[
I_{ds} = -W \mu Q_n(y) \frac{dV}{dy} + W \mu [C_{ox} [V_{gb} - V_{ddo} - V(y)] - qN_s(y)] \frac{dV}{dy}
\]

(2)

Where \( W \) is the width of channel and \( \mu \) is the carrier mobility in the inversion layer. \( \mu \) is empirically written as

\[
\mu = \frac{\mu_0}{1 + \alpha N_s}
\]

(3)

Here \( \mu_0 \) is the electron mobility of the fresh device and \( \alpha \) is the degradation factor. It was a constant in the previous work, but this assumption does not validate as shown later.

Substitute Eq.(3) into Eq.(2), multiply \( dy/L \) to both sides of the equal sign and then integrated, we get

\[
\int_{L_s}^{L_s + \alpha N_s L_{dam}} - \frac{L_s}{L_s + \alpha N_s L_{dam}} I_{ddo} - \frac{W \mu_0 N_s}{L_s} \frac{L_{dam}}{L_s + \alpha N_s L_{dam}} I_{ddo} - W \mu_0 N_s \frac{V_{ddo} L_{dam}}{L_s + \alpha N_s L_{dam}}
\]

(4)

Where \( I_{ds} \) and \( I_{ddo} \) are the drain current of damaged and fresh device respectively and \( L_{dam} \) is the damage region length. The first item at right side of Eq.(5) implies the current decrease induced by mobility degradation; and the second item reflects the impact of the interface states. Eq.(5) is also adapted to the saturation region except that \( L_{dam} \) is replaced by the effective damage region length \( L_{dam} \).

\[
L_{dam} = L_{dam} - I
\]

(6)

Here \( I \) is the pinch-off length which is calculated by the small scaled model of BSIM4.

\[
I = \frac{V_s - V_{ddo}}{E_i}
\]

(7)

Where \( V_{ddo} \) is the saturation voltage and \( E_i \) is the average electrical field in the channel.

\[
v_{sat} = \frac{2V_s - V_{ddo}}{\beta} \left[ 1 + \frac{2V_s - V_{ddo}}{\beta E_i} \right]^{-1}
\]

(8)

Where \( \beta \) is the short channel effect (SCE) factor and \( E_i \) is the field corresponding to the saturation velocity \( v_{sat} \).

\[
E_i = \frac{V_{sat}}{\mu_0} \left[ 1 + \theta(V_s - V_{ddo}) \right] \mu_0
\]

(9)

Here \( \mu_0 \) is the electron mobility at low field and \( \theta \) is the mobility attenuation factor in small scaled devices. \( \mu_0 = \frac{500 cm^2}{V s} \), \( v_{sat} = 9 \times 10^6 cm/s \) and \( \theta = 0.086 \).

The average electric field \( E_i \) is expressed as a sum of the following three items:

\[
\begin{align*}
E_i & = E_1 + E_2 + E_3 \\
E_1 & = \frac{qN_s}{2E_i \varepsilon_{Si}} (V_s - V_{ddo}) \\
E_2 & = A_2 \frac{qN_s}{\varepsilon_{Si}} (V_s - V_{ddo} - qN_s/C_{ox}) \\
E_3 & = \frac{A_3 qN_s}{\varepsilon_{Si}} (V_s - V_{ddo} - qN_s/C_{ox}) \\
\end{align*}
\]

(10)

Where \( E_1 \) is the p-n junction of drain-substrate; \( E_2 \) is the field at the edge of drain and gate; \( E_3 \) is the field at the edge of gate and inversion layer; \( A_2 \) and \( A_3 \) are empirical factors with \( A_1 = 0.2 \) and \( A_2 = 0.6 \). Combining Eqs.(5)-(10), the drain current after HCI stress is obtained.

In the reverse operation mode (exchange source and drain after HCI stress), pinch-off happened in the undamaged region, so that the drain current expression keeps the same form of Eq.(5).

\section*{3 RESULTS AND DISCUSSION}

In Eq.(5), the first item at right side implies the impact of mobility degradation, and the second item reflects the impact of the interface states. If the first item is the dominant effect, the corresponding degradation of transfer characteristic is shown in Fig.2. Concluded from the log-linear plot, \( I_{ds}-V_{gb} \) curves with different interface state density (\( N_\text{it} \)) are identified in the depletion and weak inversion region but distinct in the strong inversion region. However, if the second item dominates the degradation, the \( I_{ds}-V_{gb} \) curves are shown in Fig.3. Curves show large distinctions in the depletion and weak inversion region and come together in the strong inversion region. The above analysis is based on the constant mobility degradation factor \( \alpha \) in Eq.(3), but the result does not follow the same trend of the experimental data as shown in Fig.4.

Most experiments in our work are carried out on 15nm effective length (\( L_g \)) devices with 1.2nm sidewall thickness (\( \varepsilon_{Si} \)). The HCI stress was carried out at 2.5V drain voltage and 1.1V gate voltage with stress time from 0s to 1000s. Observed from Fig.4, in the weak inversion region, the transfer characteristic is affected by the mobility degradation (the first item of Eq.(5)); In the strong inversion region, damages at the interface are shielded by mass of inversion charges, so that the mobility recovers then the interface states (the second item of Eq.(5)).
dominated the degradation which causes the parallel shift of curves. The degradation of current is much more serious than the measured data if $\alpha$ is set to be a constant. Therefore, in our model, $\alpha$ is a function of $V_{gb}$ as $\alpha= Ae^{-BV_{gb}}$, here $A$ and $B$ are fitting parameters. With the improvement of $\alpha$, the model obtains a good match with the experimental results as shown in Fig.4.

The local distribution of interface states in the channel induced the asymmetric saturation current degradation as shown in Fig.5. Currents decrease and then rise more obviously in the forward operation mode than in the reverse mode (source and drain exchanged). The net variation of drain current is shown in Fig.6, and the model in the saturation region matches well with the measured data at different HCI stress time. Fig.7 shows the current degradation in the reverse operation mode. Saturation current declines in parallel as stress time increased.

The distinction between forward and reverse mode is because that in the forward mode, partial interface states are in the pinch-off region, so that degrade the mobility; however in the reverse mode, the damage region is near the source, the damage region is shielded by the inversion layer, so that the mobility is not affected and currents degrade
only due to the capture of the inversion charge. With the compact model in section II, the simulation result of the output characteristic in forward and reverse operation mode is shown in Fig.8.

4 CONCLUSION

This paper derived a compact model adapted to both forward and reverse HCI effect. It is concluded from the simulation and experimental results that in the weak inverse region, the degradation of carrier mobility due to interface states is the mainly impact on the current decrease; in the strong inversion region, the current decrease is determined by the capture of the inversion charge by the interface states. The compact HCI model for Nanoscale FinFET shows a very good agreement with the measured data in very operation region and mode.

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REFERENCES