

Detailed Analysis of Quantum-Effects in Nanowire Tunneling Transistors with Different Channel-Profiles

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ABSTRACT

Combining the operational principle of the tunneling field-effect transistor (TFET) with the idea of a multi-gate channel control appears as an attractive option to avoid unwanted shortchannel effects in nanometer-scale MOS-devices. In previous work we investigated the operation of various tunneling transistors using numerical device simulation and demonstrated that these exhibit a very low blocking current and an excellent on-to-off current-ratio. This motivated us to study the behavior of cylindrical and rectangular nanowire TFETs in more detail, in particular the effect of quantum confinement on the device characteristics. Specifically, we focused on potential device improvements by considering alternative materials for the gate-stack and the impact of different nanowire cross-sections on the performance.

Keywords: tunneling field-effect transistor, band-to-band tunneling, density gradient approach, numerical device simulation

1 INTRODUCTION

The progressive shrinking of the physical gate length of modern MOS-devices leads to a number of undesired shortchannel effects and, hence, the availability of alternative concepts is of increasing importance. One possible device of interest is the TFET [1], where the working principle is based on gate-controlled tunneling through a p^+n -junction. Here, the basic process is the transition of electrons and holes between the valence and the conduction energy band. In previous work we studied the operation of TFET structures on the basis of numerical device simulation and came to the conclusion that the combination of the TFET with multigate concepts may be an attractive option [2].

Fig. 1 displays the structure of a tunneling transistor in a cylindrical nanowire realization. The primary working principle of this device is gate-controlled tunneling through a heavily doped p^+n -junction. If no voltage is applied to the gate, the device behaves like a pin-diode which results in a very low blocking current. In the case of a positive voltage applied to the gate, an electron channel is induced underneath the gate. For sufficiently

high gate voltage the tunneling barrier is independent of V_{DS} , leading to an excellent saturation behaviour.

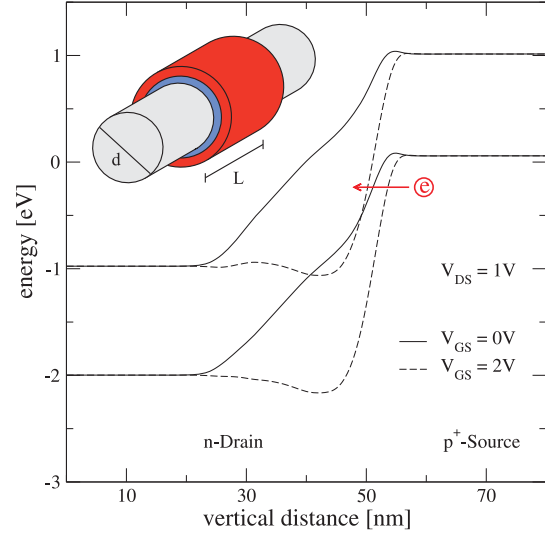


Figure 1: Energy band diagram of the cylindrical nanowire tunneling transistor at $V_{DS} = 1V$.

2 MODELING

Since phonon-assisted band-to-band tunneling and quantum confinement effects essentially determine the device characteristics, these must be properly included in the physical models used for numerical simulation.

2.1 Phonon-assisted Tunneling

Tunneling currents between strongly tilted energy bands are implemented in the formal structure of the drift-diffusion transport model by adding equivalent generation rates to the carrier source terms in the balance equations which account for the generation of electron-hole pairs in the middle of the bandgap.

Phonon-assisted tunneling is modeled on the basis of transmission probabilities which are calculated using the Kubo-formalism [4]. With the particle energy E and the electric field F this approach results in the sum of two recombination rates of the form

$$R_{pat} = B \cdot |F|^{7/2} \cdot D(F, E) \cdot \exp \left[-\frac{F_0}{|F|} \right] \quad (1)$$

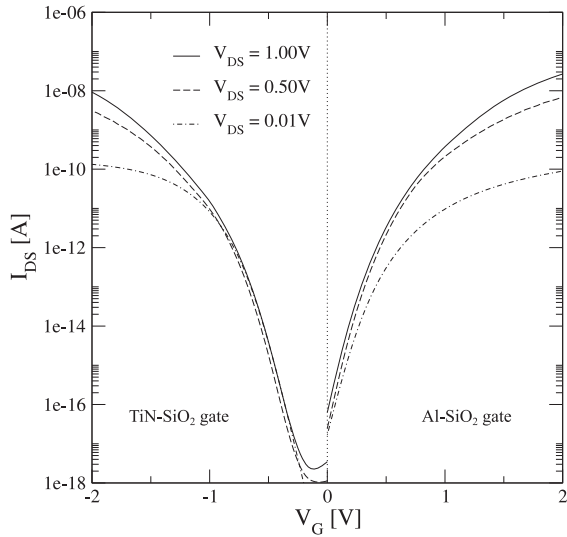


Figure 2: Simulated transfer characteristics in n- and p-operation mode.

where $D(F, E)$ depends on the Fermi-Dirac distribution functions related to the difference of intrinsic energy and the corresponding Fermi energy-levels. For numerical simulation this expression is re-written as

$$D = f_v - f_c = \frac{n_i^2 - np}{(n + n_i) \cdot (p + n_i)} \quad (2)$$

2.2 Density Gradient Approach

The quasi-classical treatment of electrons and holes in nanometer devices can be justified by introducing an additional quantum-potential [5] as correction of the quasi-Fermi levels (density gradient model)

$$\Lambda = -\frac{\gamma \hbar^2}{6m^* \sqrt{n}} \nabla^2 \sqrt{n} \quad (3)$$

with the empirical parameter γ , which is describing the relative occupation of the energy-subbands. The electron density has then the form

$$n = N_c \cdot \exp\left(\frac{E_{Fn} - E_c - \Lambda}{kT}\right) \quad (4)$$

where N_c is the conduction band density of states and E_c is the conduction band edge. The combination of both expressions results in an equation for the quantum-potential which has to be solved together with Poissons equation and the carrier transport equations.

3 SIMULATION RESULTS

Our simulations have been performed using the device simulator SENTAURUS. We studied a cylindrical nanowire TFET consisting of a 10^{19}cm^{-3} arsenic-doped drain region, opposite to a 10^{20}cm^{-3} boron-doped source region, and with a 10^{17}cm^{-3} arsenic-doped channel zone

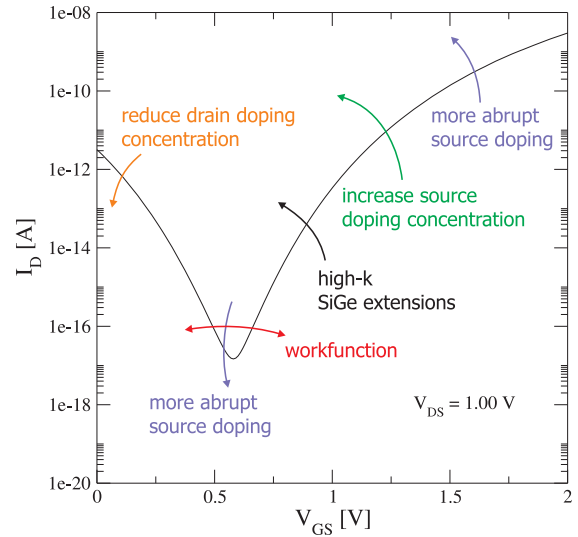


Figure 3: Optimization options for the nanowire TFET.

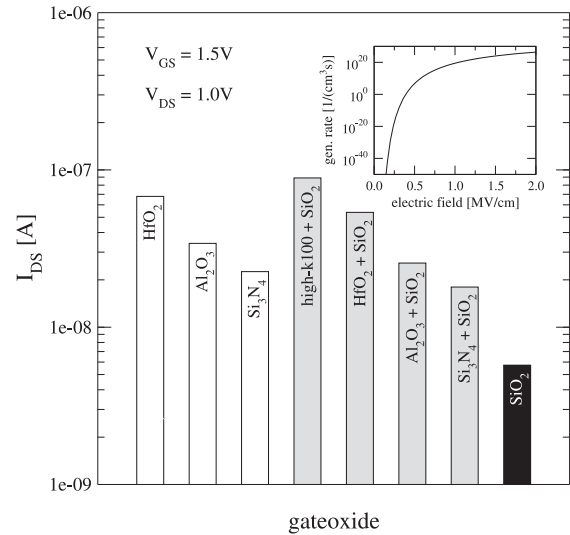


Figure 4: Simulated on-currents (at $V_{DS} = 1.0\text{V}$ and $V_{GS} = 1.5\text{V}$) of the nanowire TFET for different gate-oxide material combinations.

of 10 nm length and 15 nm diameter. The slope of the source/drain doping profiles is as steep as 2 nm/dec, and the gate stack is formed by a 2 nm SiO_2 layer and a TiN(p) or Al(n) metallization.

The resulting position-dependent energy band diagram calculated along a cutline parallel to the cylinder axis in a depth of 1 nm underneath the gate oxide for varying gate voltage (Fig. 1) demonstrates the formation of the tunneling region. The transfer characteristics of this cylindrical nanowire TFET in n- and p-operation mode are illustrated in Fig. 2. Here, n-operation mode stands for positive gate and drain voltages applied, while the source voltage is kept at zero volts. Evidently this structure exhibits a considerable on-current and in addition we find a good on-to-off current ratio with a very low blocking current.

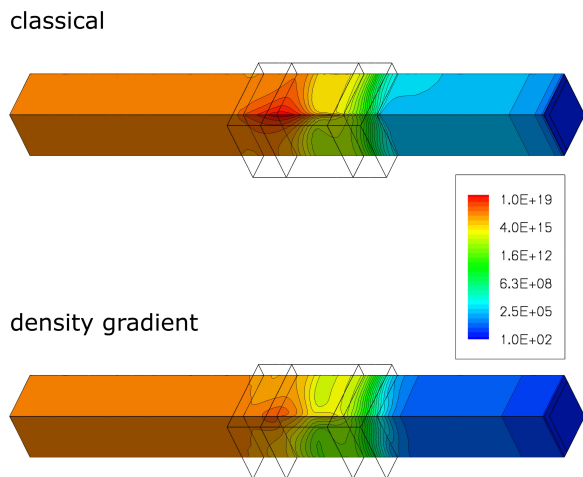


Figure 5: Electron distribution in a rectangular-shaped nanowire TFET at $V_{DS} = 1V$ and $V_{GS} = 2V$.

3.1 Optimization of Nanowire TFETs

We investigated the influence of doping variations on the device performance by analyzing nanowire tunneling transistors which have the same size and channel doping as the structure discussed above, but different drain and source doping. It is shown that varying the peak doping concentration of the extensions increases the on-current with rising doping concentrations. But, the leakage current increases accordingly. This undesired effect could be avoided by using high doping concentrations only on one side of the device. Another possible option for optimization is the use of more abrupt profiles. An overview of the different possibilities for optimizing the device performance by the design of the doping profile is shown in Fig. 3.

A further optimization of the nanowire TFET could be expected from changing the configuration of the gate stack. Changing the material of the gate metallization leads to a different workfunction which, in turn, shifts the threshold voltage. An enhancement of the on-current of the nanowire tunneling transistor can be achieved by reducing the thickness of the gate oxide. The resulting higher electric field effects an increase of the tunneling rate and, thus, of the on-current. Using high- k materials will show the same effect, but without the necessity of very thin gate oxides through which direct leakage tunneling occurs as parasitic effect. Even the combination of 0.4 nm SiO_2 and 1.6 nm HfO_2 will raise the on-current by more than one order of magnitude (Fig. 4).

3.2 Influence of Quantum-Effects

Since the tunneling current is strongly dependent on the local values of the charge densities, one expects that the source-drain current will be sensitive to quantum mechanical corrections like the density-gradient potential (see Fig. 5). This conjecture is clearly confirmed by

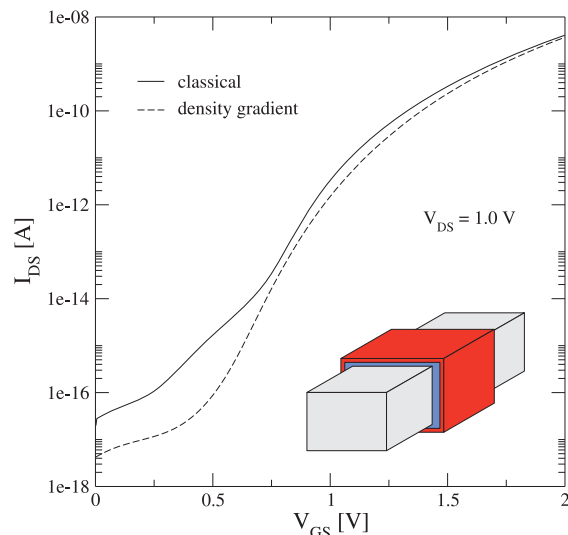


Figure 6: Effect of quantum confinement on the transfer characteristics of rectangular nanowire TFET.

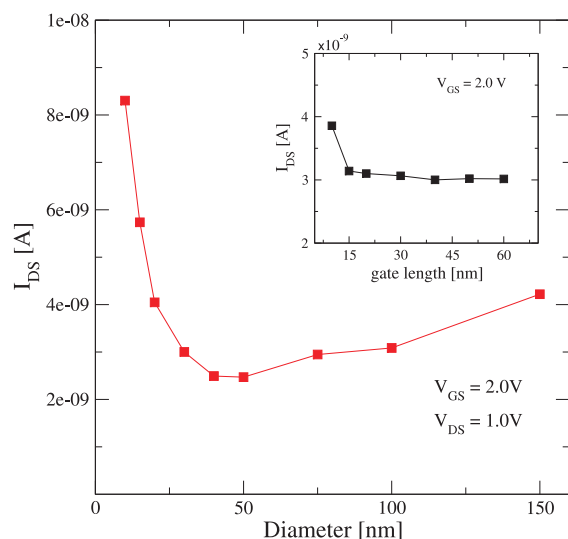


Figure 7: On-current of a cylindrical nanowire TFET in dependence of the diameter and the gate-length.

the simulated transfer characteristics. For rectangular devices this effect is even more pronounced and leads to a significant impact of quantum confinement on the transfer characteristics (Fig. 6).

3.3 Variation of the Channel-Profiles

Another crucial design parameter is the width of the channel, which is controlled by the diameter of the nanowire (Fig. 7). Starting from the minimum current value at a diameter of 50 nm, the on-current is linearly increasing with the diameter, which is easy to explain by the fact that tunneling is only possible at the source-channel interface directly underneath the gate oxide. So the tunneling region has a ring shape. Since the total tunneling rate is proportional to the cross-sectional area

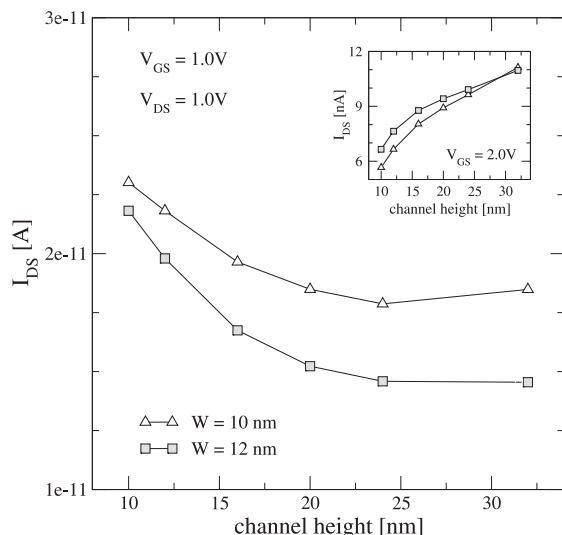


Figure 8: On- and off-current of an rectangular-shaped nanowire TFET in dependence of the channel height.

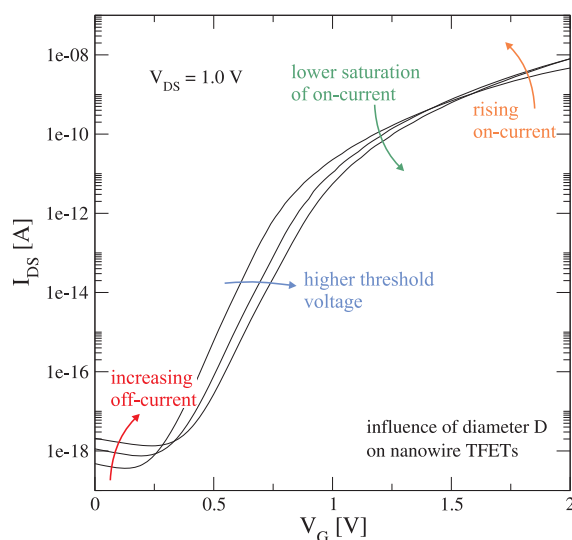


Figure 9: Influence of the channel cross-sections on the transfer characteristics of a nanowire TFET.

of the tunneling region, we end up with a linear relation between current and nanowire diameter.

The surprisingly steep increase of the current with decreasing nanowire diameter for $D \leq 40$ nm has a more sophisticated reason: In devices with small diameters the electron density is strongly enhanced, which applies in particular to the tunneling region. Consequently, this leads to a drastic increase of the tunneling rate and the resulting on-current. Due to the small width of the wire, this phenomenon extends over the complete cross-section and becomes the more pronounced, the more the diameter shrinks down.

But it has to be mentioned, that for the simulation of nanowire TFETs with a diameter below 10 nm the density-gradient method is inappropriate. Then a full quantum-mechanical treatment is necessary.

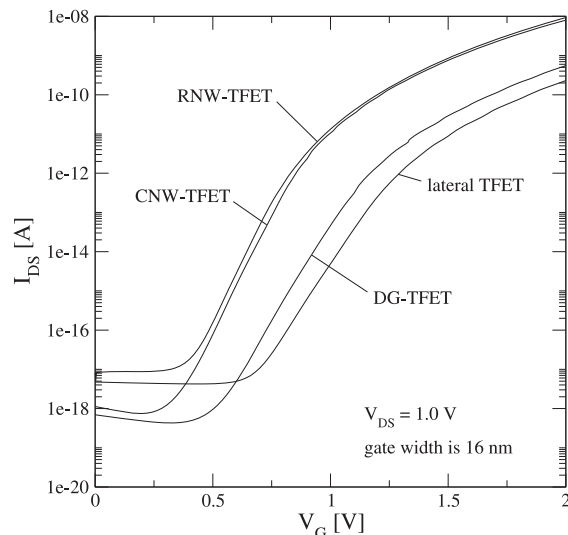


Figure 10: Comparison of the transfer characteristics of different TFETs for a gate area of 16nm \times 10nm.

As we can observe the same situation applies for rectangular nanowire TFETs (Fig. 8). Here, the effect seems to be less pronounced compared to the cylindrical transistor. But it has to be noted that the width of the rectangular TFET is still small and thus tunneling is already happening in the whole cross-section. The impact of a change in diameter on the transfer characteristics is summarized in Fig. 9. The transfer characteristics of various TFETs for an equivalent gate area are depicted in Fig. 10. We come to the conclusion that nanowire TFETs exhibit a significant gain in on-current without the necessity of higher blocking currents.

4 CONCLUSION

We demonstrated that quantum confinement effects must not be neglected in the simulation of nanowire tunneling transistors. Furthermore, downsizing of nanowire tunneling transistors will not necessarily give rise to a loss in performance. Finally we investigated the impact of different cross-sections on the device performance.

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