Fully on-chip High Q Inductors based on Microtechnologies

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ABSTRACT

This paper presents design and optimisation of SOS and MEMS inductors and compares their performance using a VCO as testbench. The paper presents the detailed analysis of effects of physical parameters of inductor structure on the Q factor and inductance in both the cases. Results showed that the 1.5nH SOS inductor achieved Q factor of 111 and MEMS inductor achieved Q factor of 45 at 4GHz frequency. Comparison of VCOs designed using these inductors show that VCO with SOS inductor achieved more than 10dBc/Hz reduction in phase noise and consumes half the power consumption compared to the VCO with MEMS inductor.

Keywords: High Q inductor, MEMS, Silicon-on-Sapphire, voltage controlled oscillator, phase noise

1 INTRODUCTION

The growing demand of wireless communications for voice and data has driven recent efforts to dramatically increase the levels of integration in radio frequency (RF) transceivers. High quality (Q) factor passive components such as inductor are the critical requirements in the design of front end blocks such as voltage controlled oscillator (VCO) and low noise amplifier (LNA) [1]. However, on-chip inductors are the bottleneck in achieving the optimum performance due to their low Q factor. The low Q factor of on-chip inductors is mainly due to the substrate losses caused by the eddy currents and inductor coil series resistance. The growing research in radio frequency (RF) systems based on alternative advanced technologies such as Silcion-on-Sapphire (SOS) and micro electro mechanical systems (MEMS) indicate that these technologies have the potential to provide a on-chip high Q inductor required in such RF systems and reduce their weight, cost, size and power dissipation [2-3]. To explore possible solutions for this bottleneck SOS and MEMS technology are investigated in this paper.

MEMS is an enabling technology and can replace most of the components in a receiver [1]. MEMS technology achieves high performance, miniaturised passive components by performing post processing steps on standard fabrication process to reduce the losses in substrate and optimises the layout parameters such as outer dimensions, width and spacing of the metal tracks, thickness of the metal and number of turns of an inductor [2]. However, this requires post processing steps which increase the cost of end product. Recently reported SOS technology, a variant of silicon-on-insulator technology, offers high resistivity substrate that has ability to considerably improve the quality factors of on-chip passive devices. Using the high resistivity substrate and thick top metal layer in SOS technology, it has been shown that with Q factors of more than 40 can be achieved for high Giga-Hz range of operation [3]. However, further optimizations at layout level can be performed to achieve even higher Q factors.

This paper presents design and optimisation of inductors using MEMS and SOS technology. A 1.5nH inductor is designed using both technologies and a VCO circuit operating at 4GHz is used as a testbench to investigate the performance improvements due to high Q factor inductors. The paper is organized as follows: section 2 and 3 present modeling, simulation and analysis of MEMS and SOS inductor respectively. Section 4 presents results along with the VCO performance and conclusion are drawn in section 5.

2 MEMS INDUCTOR

The inductor design involves understanding of effects of inductor topological parameters on the Q factor and self-resonance frequency of the inductor, design and optimisation of inductor topological parameters, choice of orientation and placement to reduce substrate effects and choice of material for the fabrication [1]. The design process involves three major design issues namely choice of topology, reduction of substrate effects and modelling the inductor performance into an equivalent circuit that effectively models the said effects.

The modelling and simulation for the MEMS inductor has been done using the Coventorware MEMS software from Coventor Inc. MemHenry Solver is employed to derive the equivalent inductor and the series resistance. The MEMS inductor is designed using copper as the material on silicon substrate. Figure 1 shows a 3-Dimentional square spiral inductor,

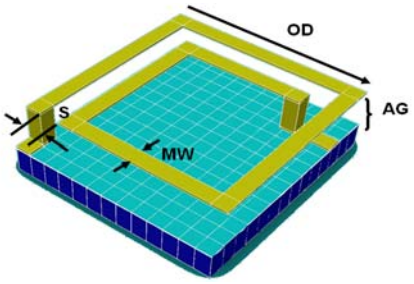

Figure 1: Structure of the spiral inductor

where OD is the outer diameter, AG is the air gap from the substrate, W is the wire width and S is the spacing between the wires of the spiral inductor.

The inductor has been analysed for the effect of air gap, metal width and spacing on inductance and Q. The variation of air gap has been fully analysed, as illustrated in Figure 2. The result revealed that inductance and Q factor increase when the spiral inductor is suspended from the silicon substrate because of the reduction in substrate losses and parasitic effects of the substrate. Figure 3 shows the effect of metal width on Q factor and inductance. From Figure 3 it can be seen that increasing the metal width will reduce the inductance and increase the peak Q factor, this is due to reduction in resistance with increasing W.

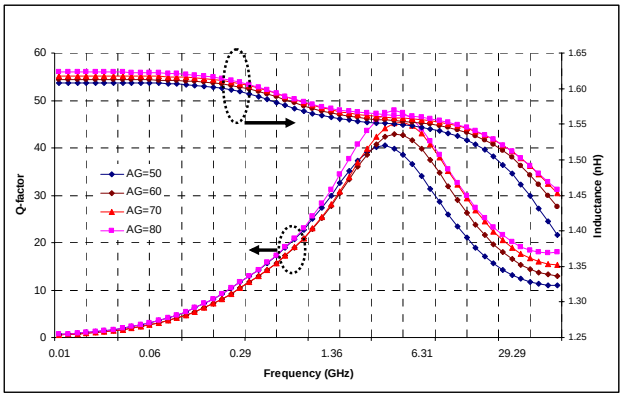

Figure 2: Effect of Air gap on Q factor and inductance [Design Parameters: OD=400µm, W=30µm, T=5µm, S=40µm]

The effect of spacing on inductance and Q factor are plotted as Figure 4. When line spacing increases, it is observed that the inductance of the spiral coil decreases. This is because as spacing increases the decrease in inductance is greater than the decrease of the series capacitance, hence the Q decreases as the spacing continues to increase.

The primary advantage of using MEMS technology is the ability to provide air gap between the substrate and the inductor coil. The introduced air gap results in reduced substrate coupling effects like eddy current losses which has negative impact on inductance value and Q factor of the inductor. However, this advantage comes at the cost of extra processing steps which increase the cost of the end product.

Silicon-on-insulator (SOI) technology can provide similar reduction in negative substrate effects due to its inherent advantage of near insulator substrate. Sillicon-on-sapphire is a variant of SOI technology that enjoys the advantage of near insulator sapphire substrate while being fabricated using low cost fabrication facilities used for standard bulk CMOS. Hence, this paper also explores the possibility of designing high Q inductors in SOS technology in next section.

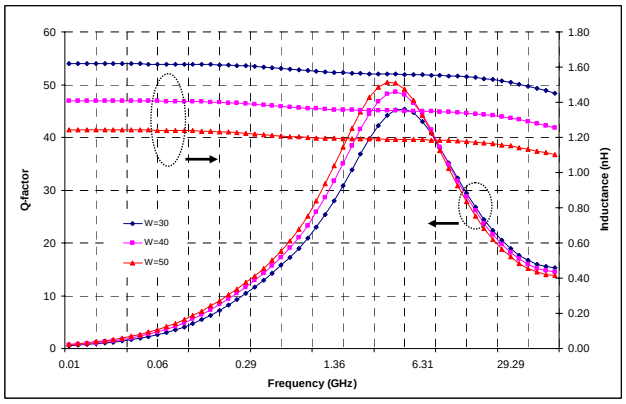

Figure 3: Effect of width on Q factor and inductance [Design Parameters: OD=400µm, S=40µm, T=5µm, AG= 70µm]

3 SOS INDUCTOR

In this paper Virtuoso Passive Component Modeller (VPCM) tool from Cadence™ was used to perform Quasi-static 3D-EM simulations and equivalent circuits were developed for each design. The key parameters for these inductor designs are outer diameter (OD) inner radius (IR), width and spacing of the metal tracks (TS), width of the metal track (TW), number of turns (NT) and the substrate material. An inductor designed in SOS technology can be best modelled using the 6 element model given in [3]. It was shown that the circular-spiral topology has highest Q factor, lowest series resistance for a similar inductance value amongst square, octagonal and circular topologies. All inductor designs use a sapphire substrate of 300µm thickness, Metal-3 as inductor coil and a patterned ground shielding in polysilicon (POLY) layer.

Analysis suggests that large inductance can be achieved by increasing the number of turns of a spiral inductor [1]. However, with the increase in number of turns peak achievable Q factor reduces due to the increase in series resistance and parasitic capacitance between the tracks. Hence, a single turn inductor can achieve maximum Q factor with largest possible operating bandwidth. Larger

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inductance can be achieved by increasing the size or the outer diameter of the inductor.

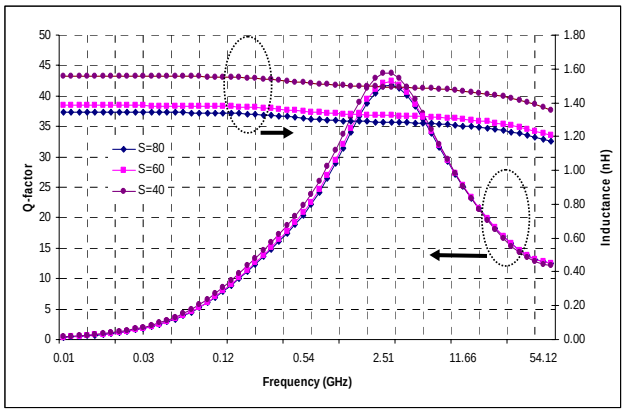

Figure 4: Effect of spacing on Q factor and inductance [Design Parameters: OD=400µm, W=30µm, T=10µm, AG=50µm]

The series resistance of the planar coil is related to the sheet resistance of the metal strip, which is inversely proportional to the width of the strip. The effects of track width on Q factor of inductor are also investigated. Figure 5 shows that with increase in track width the self-resonance frequency decreases with almost constant peak Q factor. This shows that the track width is inversely proportional to the self-resonance frequency and the operating bandwidth of the inductor. It is concluded that depending on the desired operating frequency range and bandwidth one can select the most suitable track width to achieve a desired Q factor.

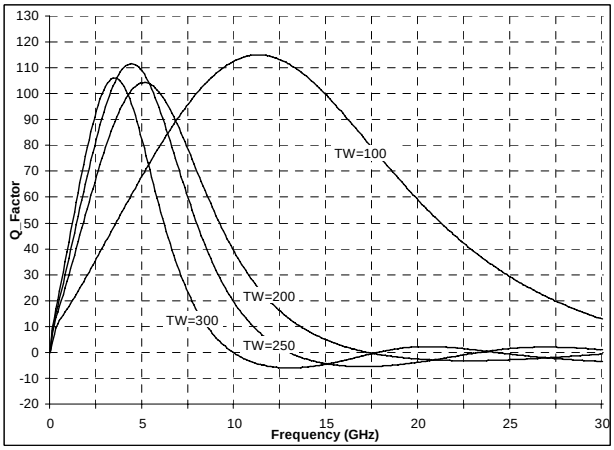

Figure 5: Track width vs Q factor [Design parameters TS=10µm, IR=35µm and NT=1]

The pattern of the ground plane can also affect the amount of eddy currents generated and it has been investigated in details in literature [4]. In an effort to further reduce the substrate coupling effects a patterned shield is introduced in POLY layer and Figure 6 shows that the Q factor can be improved by having a patterned shielding between the substrate and inductor coil.

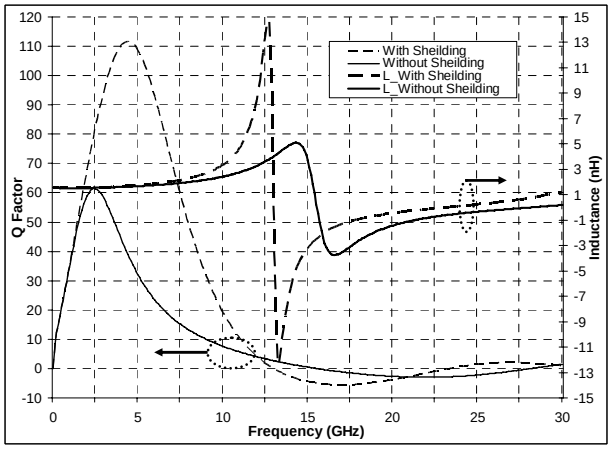

Figure 6: Presence of shielding vs Inductance and Q factor [Design parameters TW=250µm, TS=10µm, IR=35µm and NT=1]

4 RESULTS

The analysis of MEMS inductor shows that the Q factor of inductor can be improved by increasing the air gap between the substrate and the inductor coil. Results show that the required inductance of 1.5nH can be achieved with the metal width of 30µm with the various values of air gap. Figure 2 shows that the highest Q factor of 45 at 4GHz for 1.5nH inductance is achieved at air gap of 70µm. After considering the effects of various parameters on inductor performance, a 1.5nH square spiral inductor is designed with metal thickness of 5µm, metal width of 30µm, air gap of 70µm, track spacing of 40µm and outer diameter of 400µm. This design achieves an inductance value of 1.5nH with Q factor of 45 at 4GHz operating frequency as shown in Figure 7.

The inductor design using SOS technology has the advantage of near insulator substrate and added performance improvement due to use of wider metal track and patterned shielding. The final SOS inductor design achieves Q factor of 111 at 4GHz operating frequency as shown in Figure 6. The performance of the Q for 1.5nH inductors designed using MEMS and SOS technologies is compared with other literatures in Table 1. Hsiang et al [5] had designed an inductor with 2µm metal thickness, 32.1µm inner radius, 2.5 turns and 15µm metal width using 0.18µm TSMC technology. Albert et al [6] had designed spiral inductor with silicon and quartz substrates. Eun-Chul et al in [7] and Park et al in [8] presented suspended spiral inductors using surface micromachining technology with 40µm and 50µm air suspension respectively.

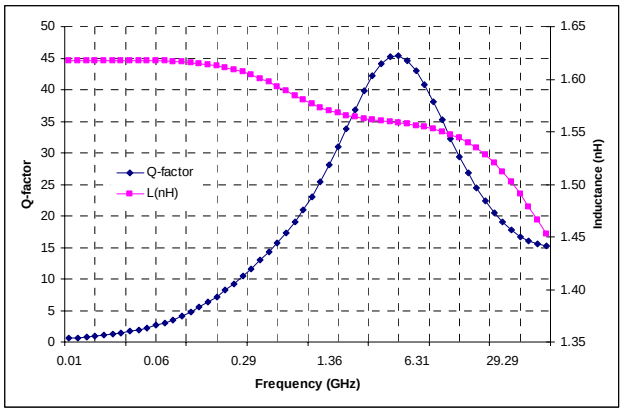

Figure 7: Inductance and Q factor of MEMS 1.5nH inductor [Design Parameters: OD=400µm, W=30µm, T=5µm, AG=70µm, S=40µm]

L (nH)	Q @GHz	NT	AG (µm)	Metal /T(µm)	S/W (µm)
1.6 [6]	12@4	2.5	80	Al/2	15/--
1.5 [7]	42@4	1.5	25	Ni/20	40/80
1.8 [8]	26@4	2.25	40	Cu/15	20/30
1.5 [9]	9@4	1.5	50	Cu/20	10/--
1.5 *	45@4	1.5	70	Cu/5	40/30
1.5 **	111@4	1	--	Cu/3.2	3/250

Table 1: Inductor design parameters and performance comparison [*This work MEMS, ** This work SOS]

4.1 VCO performance results

Cross coupled VCO architecture is the most suitable architecture for RF applications [9]. A cross coupled LC oscillator operating at 4GHz frequency is used as a testbench. The performance of VCO designed using the MEMS and SOS inductors are presented in Table 2.

Parameters	**VCO with MEMS inductor**	**VCO with SOS inductor**
Operating Voltage	2.5V	2.5V
Operating Frequency	4 GHz	4 GHz
Core Current (Icore)	10mA	4.5mA
Phase Noise 600k	-113dBc/Hz	-128dBc/Hz
Phase Noise @1M	-120dBc/Hz	-133dBc/Hz
Phase Noise @3M	-132dBc/Hz	-143dBc/Hz
Power Consumption	25mW	11.25mW

Table 2. Comparison between VCO configurations with SOS and MEMS inductors

5 CONCLUSION

This paper presents the design and implementation of inductors using MEMS and SOS technology. The inductor designs in MEMS and SOS achieve a Q factor of 45 and 11 respectively. The designed inductor improves the performance of the traditional cross-coupled Oscillator circuit. The new improved SOS inductor result in almost 10 dB reduction of phase noise with about 50% power reduction as compared to the oscillator designed with MEMS inductor. The reduced phase noise can be further traded for low power consumption for application in low power devices. A comparison of inductors in MEMS and SOS technologies suggest that the SOS has the potential to achieve higher Q factors needed for low power low cost RF applications.

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