Castellated-Gate MOSFETs as Power Transistors For Nanometer CMOS and Post-CMOS Integrated Nanosystems

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ABSTRACT

Analysis of the constant-voltage scaling characteristics of Fully-Depleted Castellated Gate (FDCG) MOSFETs reveals near term opportunities for these devices as the replacement for the "thick oxide" I/O device in CMOS System-On-A-Chip (SoC) technologies (e.g. the power transistor). Looking forward to the era of post-CMOS Integrated Nanosystems, FDCG MOSFETs utilized as PHY layer devices may provide the essential interoperable infrastructure for existing and yet-to-be-defined nanoscale devices.

Keywords: CMOS, Nanosystem, I/O, Interconnect, PHY Layer, Analog, Mixed-Signal

1 BACKGROUND

From a historical standpoint, the lineage of modern vertical dual-gate or tri-gate CMOS devices, such as the Fully-Depleted castellated-gate (FDCG) MOSFET (see Figure 1) and the presently-popular FinFET CMOS core memory/logic device, can be traced to the significant development work that has be done in the area of Silicon-On-Insulator (SOI) technology [1], discrete and integrated power devices [2,3], and notably, to the application of castellated gate structures to improve the performance of GaAs FET devices.

Some of the earliest vertical-channel FET devices which relied on fully-depleted operation were developed during the early 1980's as a way to improve the performance of discrete GaAs MESFET power transistors [4,5,6] (See Figure 2). An important result of the vertical tri-gate GaAs MESFET work was the apparent improvement in the device short-channel effect [4,5] because of the multi-gate structure.

Concisely stated, the advantage of FDCG MOSFETs as high performance analog/mixed-signal devices derives directly from their ability to deliver higher drive currents per unit area with a thicker gate oxide, and at shorter channel lengths per unit oxide thickness than a standard planer device structure.

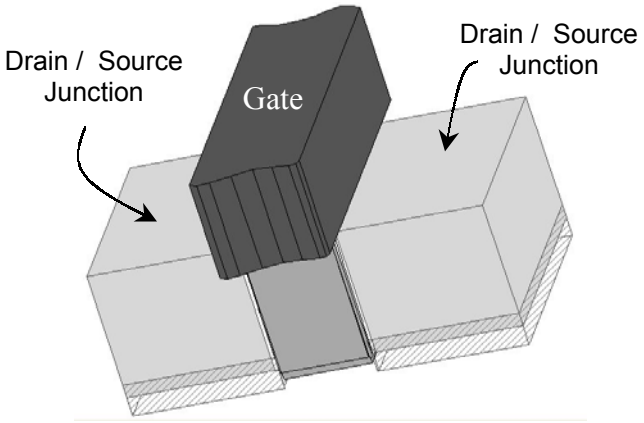

Figure 1a
Castellated-Gate (CG) MOSFET in 3D View

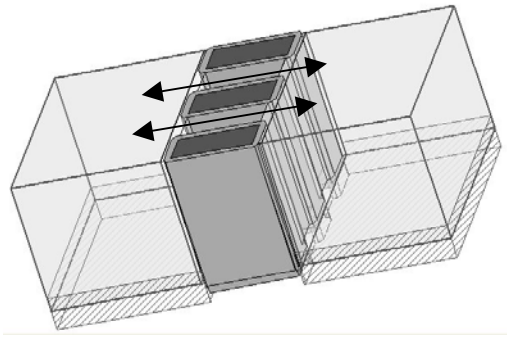

Figure 1b
CG MOSFET of Fig. 1a shown "in shadow". illustrating lateral current flow.

These operating characteristics follow directly from the area-conserving 3D structure of the device, and the improvement in threshold voltage Short-Channel-Effect (SCE) behavior as a consequence of the fully-depleted channel. Consequently, the added spatial dimension (2D=>3D) in this mixed-signal device architecture enables a constant voltage scaling mechanism with improving

performance whether the device is fully-depleted (FDCG MOSFET) or not (CG MOSFET).

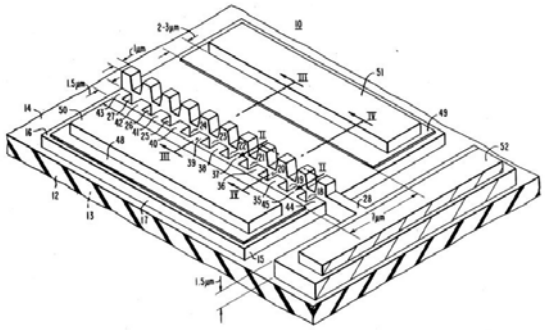

Figure 2a
Castellated Gate MESFET (from USP 4,583,107) shown in perspective view.

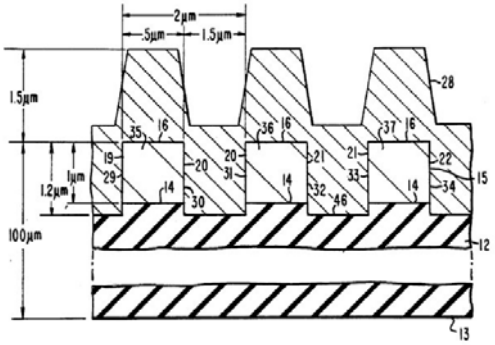

Figure 2b
Crossection of current channels from MESFET of Fig. 2a, illustrating "tri-gate" structure

2 PERFORMANCE ESTIMATES

Using a "tri-gated" device architecture as an example, the performance advantages of FDCG MOSFETs as power transistors (see Fig. 3 for definitions) can be demonstrated by performing a 1st-order comparison with a generic planar MOS device of equivalent physical area for a given voltage supply level (V_{dd}). The maximum DC / low-frequency performance improvement (F_{drv}) can be defined as the ratio of the respective device normalized-drive-currents for a given gate oxide thickness (t_{ox}), or power supply level (V_{dd}), with the result

$$F_{drv}\big|_{TG} \cong \beta \frac{n(2z+d)}{nd+(n+1)W_g} \cdot \left(\frac{L_{\min}\big|_{PSG}}{L_{\min}\big|_{TG}} \right)$$

and in the limit, for a wide device (large n)

$$F_{drv}\big|_{TG} \Rightarrow \beta \frac{(2z+d)}{(d+W_g)} \cdot \left(\frac{L_{\min}\big|_{PSG}}{L_{\min}\big|_{TG}} \right)$$

where $L_{\min}\big|_{PSG}$ and $L_{\min}\big|_{TG}$ are the minimum channel lengths of a planar single-gate MOSFET and a vertical trigate MOSFET, respectively.

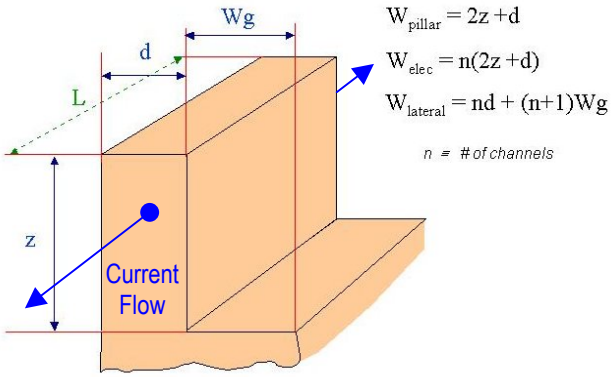

Figure 3
Dimensional definitions for a lateral current flow CG or FDCG MOSFET

The β term represents the ratio of the trigate and single-gate effective mobilities for a given threshold voltage. As illustrated in Fig. 4 , the relationships given above enable the demonstration of a constant-voltage lithography-based scaling mechanism for the nanoscale power transistor. Increasing performance can be provided, yet with gate oxide integrity-based reliability considerations intact (that is tox remains constant). For a given value of V_{ddio}, F_{drv} can potentially improve as the scaling factor increases based on a power law relationship ($F_{drv}(\lambda) \sim \lambda^{-n}$, $0.50 < n < 0.75$). Ultimately, CG/FDCG MOSFET device performance will be largely limited by thermal / power density considerations, just like it's discrete counterparts.

In addition to providing performance improvement with lithographic scaling, castellated-gate MOSFETs operating in full depletion should exhibit reduced body effect on threshold voltage. The steeper subthreshold slope of CG MOSFETs operating in full-depletion enables their operation at a lower threshold voltage for a given off-current leakage target. These two aspects operating together enable FDCG MOSFETs to provide a substantially improved power distribution function (biasing) in mixed-signal applications by reducing V_{dsat}, as well as easing the voltage translation from lower voltage "Digital Process" devices. System performance is improved since, for a given dynamic range requirement (e.g. sensor interface), power consumption can be reduced (see also [7]).

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3 NEAR TERM APPLICATIONS

While the high frequency analog/mixed-signal application of FDCG MOSFETs remains unclear [8], a number of lower frequency embedded applications exist for current and future Nanoscale CMOS platforms. One application of current interest is the use of integrated regulation to improve the energy efficiency of digital integrated circuits. In this particular application, recently demonstrated efficiency improvements [9] should be further augmented through the embedded use of CG MOSFET devices.

Another lower frequency application of embedded castellated-gate devices lies within the broad area of Mechatronics. While CG MOSFET technology is not currently at an EOS/ESD maturity level to interface directly to high power [10], it can provide a very capable interface to MEMs devices. In the sensing mode, the improved dynamic range characteristics inherent to CG MOSFETs enables one to provide pre-amplification and other signal processing functions for integrated nanosystems, without placing overly restrictive constraints on the nature of the sensor's output characteristics (a microphone, for example). In other words, your high performance MEMs sensor doesn't' have to conform to your 1V "digital process" as you pursue aggressive form factor reduction. In the "power transistor" mode, CG MOSFETs could hypothetically provide scalable high-drive capability for MEMs actuators. While at larger scales (for example a motor drive application) the power transistor would usually have to be engineered to withstand substantial Electrical Overstress (EOS), in the case of MEMs, which are typically electrostatic in operation, di/dT induced transients are of lesser concern.

4 NANOSYSTEM INTEGRATION

Within the field of microelectronics and future nanosystems, just as with many other fields, the formation of an efficient Integrated System reduces to an allocation problem. More specifically, the "success" of the resulting Integrated System often boils-down to the evaluation of Objective Functions of multi-criteria optimization, where the criteria may be measured in different units (e.g. "apples and oranges") [11]. The resulting solution(s) with respect to the objective functions is referred-to as the Pareto Optimality Tradeoff Curve, after the Italian economist Vilfredo Pareto (see Fig. 4 for example).

With the preceding methodology in mind, and looking forward to the era of nanoscale CMOS and post-CMOS Nanoelectronics, a number important observations have been made regarding the future of CMOS [12] , and the nature of integrated systems incorporating nanoscale devices [13] in terms of economics, power consumption, and the ability to connect to, or communicate with the existing system infrastructure. From an economics viewpoint, development trends for successful nanoscale CMOS technologies [14] that can effectively re-use large pre-existing design libraries demonstrate an increasing reliance on delicate manufacturing techniques [15] in order to facilitate the re-use of the existing device topologies (that is planar MOSFETs), and thereby reduce cost. By extension, future device designers should preferably have the freedom of manufacturability and backward compatibility to develop nanodevices of arbitrary complexity in order to meet their performance objectives.

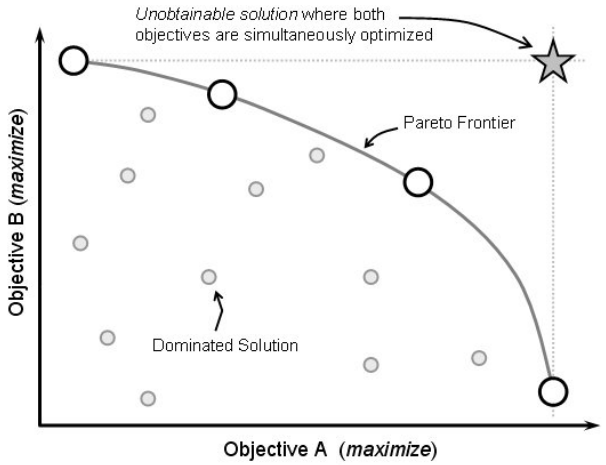

Figure 4
Illustration of Pareto Optimality Trade-Off Curve For Maximized Objectives

By proceeding to incorporate these and other factors into Objective Functions, one creates the basis to discuss the architecture of future integrated nanosystems. An architectural strategy for one specific class of semiconductor component-level Integrated Nanosystem would be to allocate the maximum "complexity" to the area-dominating nanoscale element – which is also a strategy that essentially describes CMOS technology development for the last 25 years. A 2D trade-off curve can then be defined with the addition of an Objective Function for the PHY layer / Interconnect element.

While many system designs can be economically optimized entirely through computer simulation, complex manufacturables that are the result of yet-to-be-defined processing techniques pose a much bigger problem. Therefore, in consideration of the obvious budget limitations, it will simply be argued that: To the extent that a FDCG MOSFET provides performance and/or cost improvements over it's planer counterpart, or any other device architecture of equivalent manufacturability / insensitivity to process, when incorporated within a multi-device ecosystem (System-On-Chip), *it is proposed* that the FDCG MOSFET represents a Pareto Optimal solution as a Power Transistor within an integrated semiconductor nanosystem.

5 CONCLUSION

In conclusion, Fully-Depleted Castellated-Gate (FDCG) MOSFET devices can offer a number of substantial performance improvements over existing approaches for future nanoscale System-On-Chip technology platforms. The introduction of nanoscale feature sizes in the I/O or power function demonstrates the opportunity for increasing net performance with shrinking feature size. Finally, the ability of the device to be unobtrusively integrated in an arbitrary multi-device SoC ecosystem translates into the possibility that the FDCG MOSFET may provide a Pareto Optimal PHY Layer and/or power management solution for future classes of integrated nanosystems.

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