Quantum Dot (QD) gate Si-FETs with Self-Assembled GeO$_X$ Cladded Germanium Quantum Dots

*M. Gogna, *F. Al-Amoody[*], *S. Karmakar, **F. Papadimitrakopoulos[**], and F. Jain[*]

[**]*Chemistry Department and Institute of Materials Science*
[*]*Electrical and Computer Engineering Department, University of Connecticut, 371 Fairfield Road, Storrs, CT 06269-2157*
Phone: 860-486-3752, fax 860-486-2447.
Contact email: fcj@engr.uconn.edu

1 ABSTRACT

This paper presents preliminary data on the transfer and output characteristics of a GeO$_X$-cladded Ge quantum dot (QD) gate Si MOSFET. The MOSFET is formed by depositing cladded QDs above the SiO2 gate insulator formed on p-Si region, sandwiched between n-type source and drain. Ge (~ 2 to 8 nm) nanoparticles, cladded with GeO$_X$ (~1nm) layers, are deposited using site-specific self-assembly. In addition, threshold shift in a nonvolatile memory structure, having cladded Ge dots, is also presented. The aim here is to fabricate floating QD gate high performance nonvolatile memory scalable to 22 nm processing.

Keywords: Quantum dot gate FETs, Cladded quantum dot, Ge quantum dot gate FETs.

2 INTRODUCTION

Quantum dot nonvolatile memories were first reported by Tiwari et al [1]. Since then there has been significant interest in QD gate devices.
Nanoscale germanium has also attracted considerable interest for the applications in photonics, optoelectronics, and hybrid composite materials. For example, a GeO$_2$ quantum dot is a blue photoluminescence material with weak peak energies around 3.1 eV and 2.2 eV [2, 3]. One-dimensional GeO$_2$ quantum wires offer excellent optical properties [2]. In quantum dots, the electronic and optical properties are strongly depend on their size and dimensionality. However, the sizes of the germanium oxide quantum dots or quantum wires in literatures were always more than 100 nm.

We present synthesizing smaller Ge nanoparticles (~2 to 8nm) cladded with GeO$_x$ that can be used for various device applications. We have obtained GeO$_X$-Ge nanoparticles with core diameter of 4 and 8 nm.

The influence of dot diameter on the performance of FETs and floating quantum dot gate nonvolatile memory (QDNVM) is under further investigation.

3 SYNTHESIS OF GeO$_x$-Cladded Ge QUANTUM DOTS

Germanium quantum dots are synthesized by ball-milling of polycrystalline germanium powder (99.999% purity) obtained from Alfa Aesar. High energy ball-milling is performed in a round-ended hardened steel vial with steel balls. After milling, the nanomilled germanium powder is mixed with an oxidative agent solution in a sealed flask and sonicated for 2 days while maintaining its pH between 5 and 5.5. The germanium nanoparticles (with average particles size of 20 nm core and 1 nm cladding)are then separated by centrifuging the solution at 3000, 6000, 9000 and 13000 RPM. The size of the GeO$_X$-Ge nanoparticles can be further reduced to form 4 nm and 8 nm quantum dots.

Figure 1(a) shows site-specifically self-assembled cladded Ge dots on a p-Si surface having a thin SiO2 layer. The p-Si regions are separated by n-Si regions (which are obtained by selective diffusion of phosphorus via a SiO$_2$ mask). The site-specifically self-assembled GeO$_x$-Ge films are characterized by an Atomic
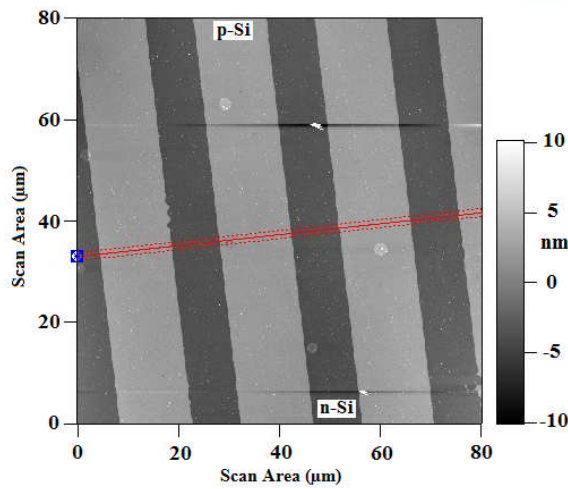
Force Microscopy (AFM) as shown in figure 1(b).

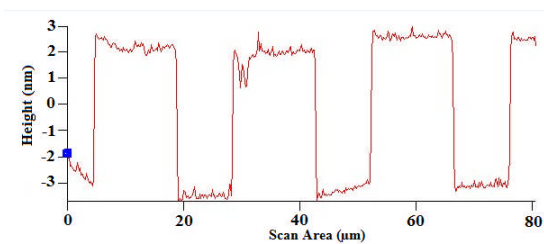Figure 1(a). Site-specific self-asembly of monodispersed GeO$_X$-Ge quantum dots on 10 micron p-Si.

Figure 1(b) AFM surface profile for GeO$_X$-Ge deposition in Figure 1(a)

4   QUANTUM DOT GATE FETs

Figure 2 shows the cross-sectional schematic of a GeO$_x$-Ge QD gate Si FET. Here, the QD gate is implemented by forming layers of monodispersed GeO$_x$-Ge (4nm) dots using site-specific self-assembly [4] which preferentially deposit on the p-doped channel region [between the n-doped source and drain]. The dots are assembled on a thin layer of SiO$_2$.

Figures 3(a) and 3(b) show the transfer and output electrical characteristics of a fabricated QD gate Si FETs using GeO$_x$-Ge QDs.
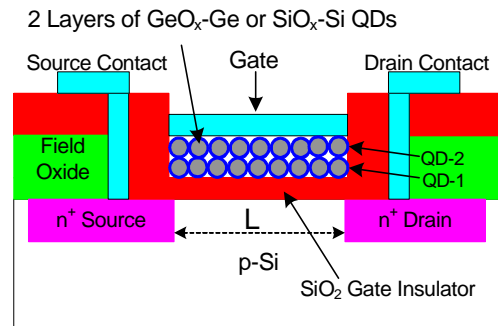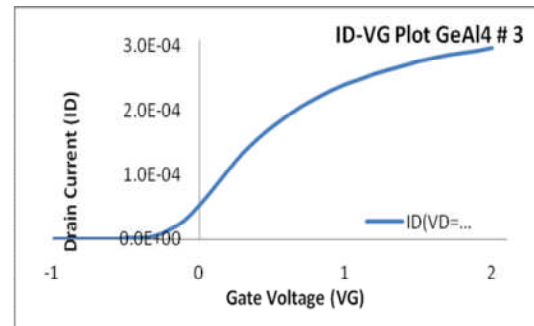

Fig. 2 Cross-sectional schematic of a GeO$_x$-Ge QD gate FET.

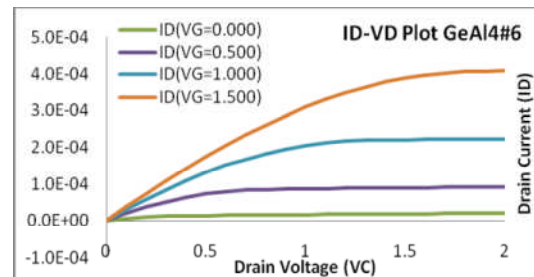Figure 3(a): Transfer ID-VG characteristic of GeO$_x$-Ge (2-4nm) quantum dot gate Si-FET device.

Fig 3(b): Output ID-VD characteristics for quantum dot gate Si-FET device.

5   QUANTUM DOT GATE NONVOLATILE MEORY

Figure 4 shows the transfer characteristics of a nonvolatile memory using GeO$_x$-Ge cladded dot as the floating gate. In contrast to the FET device of Fig. 3, the nonvolatile memory structure has a control gate insulator layer (Si$_3$N$_4$ ~75 Angstroms). Earlier, our group reported [5] fabrication of QD gate memories using SiOx-cladded Si dots.

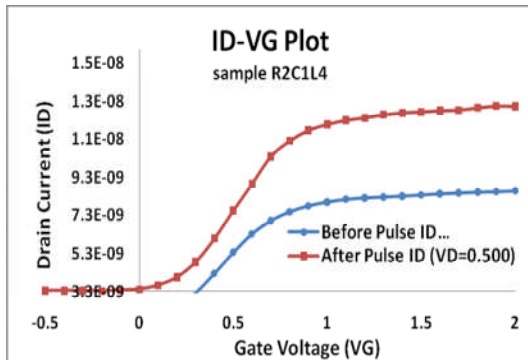The threshold shift was obtained by applying an electrical pulse (3V, 1msec) at the drain while keeping the gate at 5V.

Fig. 4. Transfer characteristics of GeO$_x$-cladded Ge quantum dot floating gate nonvolatile memory.

6 CONCLUSION

We have presented experimental results on fabricated FETs and nonvolatile memory devices where GeO$_x$-Ge monodispersed cladded dots are used in the gate region. The memory device shows an appreciable shift in the threshold. The influence of dot diameter on the performance of FETs and floating quantum dot gate nonvolatile memory (QDNVM) is under current investigation.

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4. F. C. Jain and F. Papadimitrakopoulos, Site-specific nanoparticle self-assembly, US Patent 7,368,370, 2008.
5. R. Velampati, and F. C. Jain, A Novel Nonvolatile Memory Using SiOx-Cladded Si Quantum Dots, NSTI Nanotech , Santa Clara, CA, May 20-24 2007.