Electrical Characteristics of Nanoscale Multi-Fin Field Effect Transistors with Different Fin Aspect Ratio

Hui-Wen Cheng, Chih-Hong Hwang and Yiming Li*

Department of Communication Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan; *Email: yml@faculty.nctu.edu.tw
Phone: 886-3-5712121 ext. 52974; Fax: 886-3-5726639

ABSTRACT

Device characteristics of multiple-fin silicon field effect transistors (FETs) are sensitive to the channel fin aspect ratio (AR = the fin height / the fin width). In this study, dependence of characteristics on AR for single- and multi-fin FETs are examined by using a three-dimensional device simulation. The threshold voltage ($V_{th}$) variation of triple-fin FET is smaller than that of single-fin one due to a relatively larger effective device width. The triple-fin device with FinFET structure (AR = 2) exhibit rather stable $V_{th}$ roll-off characteristics owing to more uniform potential distribution inside the channel. The results of our study show that the driving current, transconductance, gate capacitance of FinFETs are superior to that of tri-gate (AR = 1) and quasi-planar (AR = 0.5) FETs. From the layout viewpoint, FinFETs has the best layout area efficiency; consequently, to design a device with the subthreshold swing < 70 mV/dec, the layout area of FinFETs is 1.67 and 1.33 times smaller than those of quasi-planar and tri-gate FETs.

Keywords: Channel Fin, Characteristic Sensitivity, Aspect Ratio, FinFETs, Tri-Gate FETs, Quasi-Planar FETs, 3D Device Simulation.

1 INTRODUCTION

As the gate length of bulk metal oxide semiconductor field effect transistor (MOSFET) shrinks below 45 nm, the fundamental physical limitation is approached gradually, for example, such as serious short channel effects (SCEs), the performance degradation due to increasing access resistance, and limitations of conventional gate stack and other technological difficulties. Those choke points limit the conventional bulk MOSFETs to scale. In order to enhance the controllability of channel to continue scaling according to Moore’s Law beyond the 32-nm technology nodes, diverse approaches have been proposed, such as the usage of strain silicon [1], high-$\kappa$ dielectrics [2] and metal gate technology [3], and change of the device structure. Among these promising techniques, the MOSFET with multiple-gate structures, such as the fin-type FETs (FinFETs) have start to drawn people’s attention due to the good suppression of SCEs, high transconductance ($g_{m}$), ideal subthreshold swing (SS). Moreover, high aspect ratio tri-gate FinFETs with aggressively scaled fin widths (e.g., 10 nm and narrower) are of particular interest as they combine excellent SCE immunity with high drivability per unit chip area. In this work, a three-dimensional (3D) quantum drift-diffusion device simulation [4] is conducted on our parallel cluster system [5-6] to explore the electrical characteristics of vertical channel device with different geometric aspect ratio through the dependence of SCEs of transistors on the device dimensions. To ensure the best accuracy, the used physical models of the explored device have been carefully calibrated with experimental data.

This article is organized as follows. Section II describes the simulated devices. In section III, the characteristic sensitivity is compared between single-fin and multi-fin structures with different AR. Finally, we draw the conclusions in Section IV.

2 THE STRUCTURE AND SIMULATION

![Figure 1: (a) A 3-D schematic view of multi-FinFET, where Lg, Tsi and Wsi stand for the gate length, fin height and fin width. (b) A cross-section view of fin which are FinFET (AR=2), tri-gate (AR=1) and quasi-planar (AR=0.5) respectively.](image)

Fig. 1: (a) A 3-D schematic view of multi-FinFET, where Lg, Tsi and Wsi stand for the gate length, fin height and fin width. (b) A cross-section view of fin which are FinFET (AR=2), tri-gate (AR=1) and quasi-planar (AR=0.5) respectively.

Fig. 1(a) shows the structure of studied 3D triple-fin transistor, where the silicon oxide is 1.2 nm, the channel doping concentration is $1.48 \times 10^{18}$ cm$^{-3}$ and statistically generated discrete dopants. Transistors with different aspect ratio (AR = the fin height / the fin width) of fins are
simulated, where the AR of FinFETs, tri-gate MOSFETs, and quasi-planar MOSFETs are two, one and 0.5, as shown in Fig. 1(b), respectively. The different AR could reflect the different gate-control-capability and benefit the design of FETs with vertical channel structures. To investigate the suppression effectively of SCEs and sensitivity of intrinsic device parameters for the explored transistors, the gate lengths of devices are varied from 32 nm to 16 nm and the fin widths of devices are varied from 16 nm to 8 nm. The device characteristics with and without random dopants are obtained by solving a set of 3D quantum corrected transport equations, under our parallel computing system [5-6]. The physical models adopted in the device equations have been calibrated with the fabricated and measured samples for the best accuracy [4,7-9].

3 RESULTS AND DISCUSSION

Figures 2(a) and 2(b) show the gate-length-variation-induced $V_{th}$ deviation ($\Delta V_{th}$) for the single- and triple-fin transistors with respect to different AR. The $V_{th}$ deviation is defined as the difference of $V_{th}$ between the nominal case (i.e., the 16-nm-gate-length) and process variation altered cases (they could be 14.5-nm- or 17.5-nm-gate-length), as shown in the inset of Fig. 2(a). The results show that $V_{th}$ deviation of the triple-fin device is significantly smaller that of single-fin one. For the FinFET, the $V_{th}$ variations of triple-fin FinFET is 1.64 times smaller than that of single-fin one, in which the three sigma of the gate-length-variation including the line-edge-roughness, and the gate-length-deviation is about 1.5 nm according to the International Technology Roadmap for Semiconductors (ITRS) [10]. It has also been found that the FinFET possesses the smallest $V_{th}$ variations among the explored devices due to a more uniform potential distribution and well channel controllability, as shown in Fig. 3. For the FinFET and the quasi-planar device with a similar effective channel width, the potential difference inside the FinFET’s channel is about 1.5 times smaller than that of quasi-planar device. For single-fin transistors, the $V_{th}$ variations of FinFET are 1.42 and 1.78 times smaller than those of tri-gate and quasi-planar FETs. The normalized $V_{th}$ variation for the single- and triple-fin FETs are summarized in Table 1, where the normalized $V_{th}$ variation is defined as the difference of $V_{th}$ between the 14.5-nm- and the 17.5-nm-gate lengths divided by the nominal $V_{th}$.

![Potential (mV)](image)

Figure 3: The potential distribution for the FinFET with the 8-nm-width fin and the quasi-planar with the 16-nm-width fin, where the gate length is 16 nm.

![Table 1](image)

Table 1. The normalized $V_{th}$ variation of quasi-planar, tri-gate and FinFET devices for single- (I) and triple-fin (II), where the $V_{th}$ variation is defined as the difference of $V_{th}$ between the 14.5-nm- and 17.5-nm-gate lengths. The $V_{th}$ variation is then normalized with respect to the nominal $V_{th}$ of 150 mV.

\[
\begin{array}{ccc}
\text{AR} & \text{AR = 0.5} & \text{AR = 1.0} & \text{AR = 2.0} \\
\text{I} & 33.3\% & 26.7\% & 18.7\% \\
\text{II} & 27.3\% & 20.0\% & 11.3\% \\
\end{array}
\]

\[
W_{eff} = n(2H_{fin} + W_{fin})
\]

(1)

and

\[
I_D = \frac{n(2H_{fin} + W_{fin})}{L} \mu C_{ox}(V_G - V_{th})^2
\]

(2)

where $n$ is the number of fins, $W_{eff}$ is the effective fin width for multi-gate devices, $H_{fin}$ is the height of fin, $C_{ox}$ is the capacitance of per unit gate area, $L$ is the gate length, $\mu$ is the mobility, and $V_G$ is the gate voltage. From Eq. (1), the effective fin width is increased as number of fins is increased. As depicted in Eq. (2), the on-state current of
transistor increases as the number of fin increases, and therefore the driving capability of the triple-fin transistor is larger than that of the single-fin device. The triple-fin transistor can possess better immunity against fluctuation and have a larger driving current to benefit the high performance applications. The \( V_{\text{th}} \) roll-off characteristics for triple-fin MOSFETs are then investigated from different AR viewpoint, as shown in Fig. 4, in which the fin width varies from 8 nm to 16 nm and the device gate length varies from 32 nm to 16 nm. For quasi-planar MOSFETs with 16-nm-width triple-fin (the dash line with the square open symbols), the \( V_{\text{th}} \) decrease from 0.3 V to 0.093 V, as shown in Fig. 4. The \( V_{\text{th}} \) difference is about 96%. And the reduction of \( V_{\text{th}} \) with 8-nm-width triple-fin is about 45%. The tri-gate MOSFET and FinFET also exhibit similar characteristics. The results reveal that the transistor with a thinner fin width may show less \( V_{\text{th}} \) roll-off characteristics due to the well gate-control of fully-depleted channel. The \( V_{\text{th}} \) roll-off differences between the wide device (16 nm) and the narrow one (8 nm) are increased with decreasing AR, which indicates the requirement of narrow width structure for MOSFETs with small AR design. However, we would like to mention that for devices with narrow width, its effect will be enhanced and introduce another source of fluctuation in the threshold voltage. Comparing triple-fin transistors with different aspect ratio, the FinFET structure possesses a smallest \( V_{\text{th}} \) variation, where the transistors with a thick fin width exhibit a larger on-state current due to the decrease of channel resistance. The on-state current of the 16-nm-fin-width transistor is about two times larger than that of the 8-nm-fin-width device. The relation between the driving current and AR could be estimated by

\[
I_D = \frac{n(2 \cdot AR + 1) \cdot W_{\text{fin}} \cdot \mu C_{\text{ox}}}{L} (V_G - V_{\text{th}})^2. \tag{3}
\]

The device with a higher aspect ratio may have a larger on-state current. The conducted I-V curves also verify Eq. (3), where FinFETs has a higher on-state current. Though the increase of transistor's fin width may enhance the driving capability, the wider fin width of transistors also may lose the channel controllability and then degrades the device performance, as shown in Figs. 5 and 6. Fig. 5 shows that the triple-fin FinFET with 16-nm-gate-length and 8-nm-width-fin shows a larger ratio of the on/off current, which is about 1.94 and 4.43 times larger than those of tri-gate and quasi-planar MOSFETs. Fig. 6 shows that the transconductance \( g_m \) of the explored devices increases as the gate length scales. And the device with thinner device exhibits a smaller \( g_m \) due to the smaller driving current. For devices with different AR, the triple-fin FinFET of 16-nm-gate-length and 8-nm-width-fin shows a larger ratio of the on/off current, which is about 1.36 and 2.28 times larger than those of tri-gate and quasi-planar MOSFETs, according to the estimation of Eq. (2). For FinFETs, the requirement on the height of the fin to obtain a competitive layout density is achieved; for example, to design a device.
with the SS < 70 mV/dec, the layout area of FinFETs is 1.67 and 1.33 times smaller than those of quasi-planar and tri-gate structures, as shown in Fig. 7. The FinFETs may possess a better channel controllability, higher driving current and better layout efficiency than transistors with smaller aspect ratio.

4 CONCLUSIONS

In this study, characteristic sensitivity of multi-fin FETs to channel fin aspect ratio was examined using a 3D device simulation. Triple-fin FinFETs have about 1.64 times smaller $V_{th}$ variation than that of single-fin one. Device with narrower channel width may exhibit an even smaller $V_{th}$ fluctuation because of uniform potential distribution inside the device channel. Reduction of $V_{th}$ variation for the triple-fin FinFET is 1.76 and 2.41 times smaller than those of tri-gate and quasi-planar structures. For 32 nm – 16 nm multi-fin FETs with 8-, 12- and 16-nm-width fins, the FinFET also possesses the largest driving capability, the largest gm. For devices with 16-nm-gate length and 8-nm-fin width, the driving current, the on/off current ratio and the gm are 2.24, 4.43 and 2.28 times larger than those of quasi-planar MOSFETs. In design of multi-fin transistors, the device with narrower channel width exhibits an even smaller $V_{th}$ fluctuation because of the more uniform potential distribution inside channel. Moreover, the narrow width effect will be enhanced and introduce another source of fluctuation in $V_{th}$. Besides the transistor’s characteristics, from the layout viewpoint, the FinFETs shows the best layout area efficiency due to its better channel controllability. To design a device with the SS < 70 mV/dec, the layout area of FinFETs is 1.67 and 1.33 times smaller than those of quasi-planar and tri-gate FETs.

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