ChiralMEM: A Novel Concept for High Density Magnetic Memory Technology

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ABSTRACT

ChiralMEM is a new concept for high-density magnetic random access memory for information technology [1-3]. It is an array memory capable of storing multiple bits of information per array cell in contrast to conventional existing single-bit-per-cell technologies. ChiralMEM is based upon the creation of multiple magnetic states by chirality dependant selective pinning of magnetic domain walls. Importantly, ChiralMEM is compatible with existing fabrication technology.

Keywords: MRAM, spintronics, domain walls, multi-bit cell, nanowire

1 BACKGROUND

Magnetic random access memory (MRAM) is a type of solid-state magnetic memory technology that brings together nanomagnets and spintronics in a technology that entered the market place in 2006. MRAM has been described as the ‘ideal’ or ‘holy grail’ of memory that brings together the high memory density of DRAM with the data input and output speed of SRAM, the non-volatile capability of Flash memory (needing no power to maintain the memory) and unlimited rewrite endurance [4].

MRAM stores information using the magnetization direction of nanomagnets. For memory applications MRAM cells are fabricated in large arrays with individual memory cells located at each intersection (node) between orthogonal conductors within the array, see fig. 1a. Each cell is composed of a multilayer structure with a fixed magnetic layer, dielectric layer and a free layer usually based on a NiFe alloy. The magnetization direction of the free layer can be switched to one of two directions in response to a localised magnetic field, see fig. 1b. The magnetic field needed to switch the magnetization direction (‘write’) of the free layer is generated locally by the flow of current through lithographically defined wires called the word- and bit-lines. In conventional MRAM the dimensions of the magnetic structures are such that they are composed of areas of uniform magnetization, called single domains.

Stored data is read-out from the structure by measuring the electrical resistance vertically through the multilayered MRAM structure, see fig. 1c. The resistance through the stack depends upon the relative orientation of the two magnetic layers. When the magnetization within the free layer and the reference layer are parallel the resistance is low and conversely, when the magnetization directions within the two layers are anti-parallel the resistance is high. The dielectric layer acts as an electrically insulating barrier between the metallic magnetic layers. Current flows through this barrier when a bias voltage is applied to the cell during readout, through the quantum mechanical process of electron tunneling. This structure is referred to as a Magnetic Tunnel Junction (MTJ). Simplistically, the resistance depends on the electron spin states either side of the junction [5].

The architecture of each memory cell is referred to as 1T1MTJ (one transistor and one magnetic tunnel junction per cell) and has been developed and utilized in the first commercial MRAM product, a 4Mb memory chip produced by Freescale Semiconductor Inc. [6] and was also used in the 16Mb chip demonstrated by the MRAM Development Alliance (IBM – Siemens collaboration) [5].

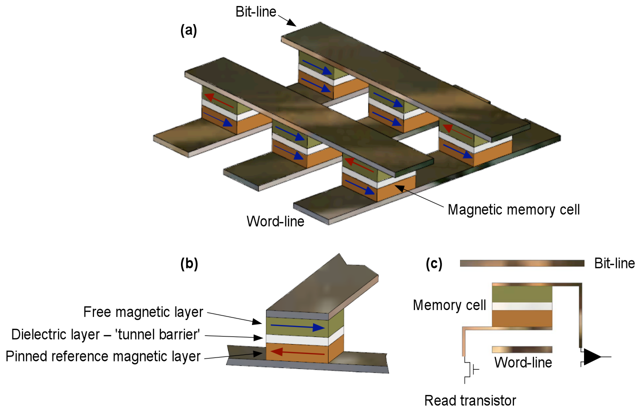

Figure 1: (a) Overview of simplified MRAM array. (b) Schematic of single MRAM cell showing fixed ‘pinned’ reference layer and the switchable data storage ‘free-layer’ separated by a dielectric ‘tunnel barrier’ forming a magnetic tunnel junction (MTJ). The resistance of the MTJ is either high or low depending on the direction of the free layer magnetization with respect to the pinned layer. (c) Schematic illustration of the MTJ resistance measurement arrangement. The readout transistor is patterned into the CMOS circuit and the magnetic structures are fabricated on top as a back-end module.

Within the 1T1MTJ architecture the MTJ is connected in series with a CMOS FET (complimentary metal oxide semiconductor field-effect transistor) see fig. 1c. The FET is used to select a cell when reading out the memory state. This architecture has important benefits particularly for read-out. But critically, the relatively large size of the CMOS components leads to low memory density for arrays of conventional single bit per transistor technology.

To remain competitive, memory technologies must be scalable, taking advantage of developments in lithographic technology. This is driving research into alternative approaches to increase MRAM storage density.

Utilizing ever-smaller cells is hampered by the physical limitation imposed by the superparamagnetic threshold, the particle size below which the magnetization of the cells will be capable of spontaneously reversing as a result of thermal fluctuations. Storage density could also be improved by increasing the number of memory states that can be stored in a single magnetic nanowire. By including structural features in magnetic nanowires, it is possible to produce a structure that can exist in a number of different magnetic states each of which can represent data bits.

2 THE ChiralMEM CONCEPT

The ChiralMEM concept will create a multi-bit memory cell capability that can be integrated with conventional MRAM to produce a higher data storage density RAM. The capacity of ChiralMEM to store multiple data bits in a single cell will be achieved by controlling the selection of one of a number of multiple magnetic states in an elongated ferromagnetic nanostructure. In planar nanowires made of polycrystalline permalloy ($Ni_{81}Fe_{19}$) the magnetization is constrained by magnetostatic energy considerations to lie along the long axis of the wire with spins parallel to the surfaces and edges. The lowest magnetic energy state occurs when the magnetization is uniform along the wire axis. If a magnetic field of opposite polarity and adequate strength is then applied to the wire, magnetization reversal of the nanowire will occur. Magnetization reversal in nanowires occurs by the formation of a reversed magnetic domain and an associated boundary, called a magnetic domain wall, between the oppositely directed domains. This wall then propagates through the wire, completely reversing the magnetization. The formation and initial position of a domain wall can be controlled by a larger ‘nucleation-pad’ at one end of the nanowire, see for example fig. 2. Due to its shape, the magnetization of the nucleation pad will reverse before the magnetization in the wire in the presence of an axial magnetic field. This results in a domain wall forming at the junction between the nucleation pad and the wire. The domain wall will pin at this junction until the applied field is strong enough to give the domain wall enough energy to propagate down the wire.

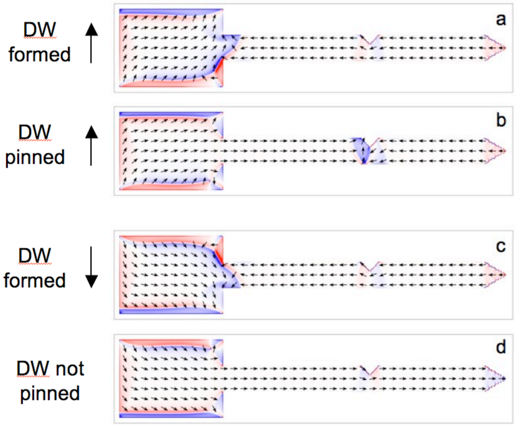

Figure 2: Micromagnetic simulations showing the behavior of domain walls with different magnetization configurations (a) The formation of a transverse wall with magnetization pointing upwards and (b) pinning of the wall at the notch for applied axial fields up to 60 Oe. (c) The formation of a transverse wall with magnetization pointing downward and (d) the domain structure at 45 Oe where the wall propagates past the notch and is swept out of the wire.

Similarly the domain wall can also be pinned by other structures that it encounters along the wire. The presence of an adequately large notch in the wire will pin the domain wall, where it will remain until the applied magnetic field is strong enough to give the domain wall the energy to de-pin and continue moving along the wire, fig. 2. The micromagnetic simulations use the OOMMF code from NIST [7].

The key physics being exploited for the first time is that domain walls are not symmetrical physical objects but have a micromagnetic structure that depends on the sense of rotation (chirality) of the electronic spins that form the domain wall. The micromagnetic structure of domain walls varies, depending on the thickness and width of the wire from transverse walls in thinner/narrower wires to vortex walls in wider and thicker nanowires [8]. In a transverse wall the spins are largely in plane and at the centre of the wall the spins point at 90° to the wire axis, in one of two directions, see fig. 3. For vortex walls the domain wall has a circular structure and the sense of rotation of the spins is either clockwise or counter-clockwise. Hence each wall type can exist in two chiralities.

In symmetrical nanostructures the two chiralities of each domain wall type are energetically equivalent, and symmetrical features, such as paired notches on opposite sides of a wire, present the same energy barrier to both possible magnetization configurations. However an asymmetric structural feature, such as a single notch on one side of the wire, (e.g. fig. 2) will present different energy barriers and hence pinning fields to propagating domain walls depending upon the chirality of the wall [1].

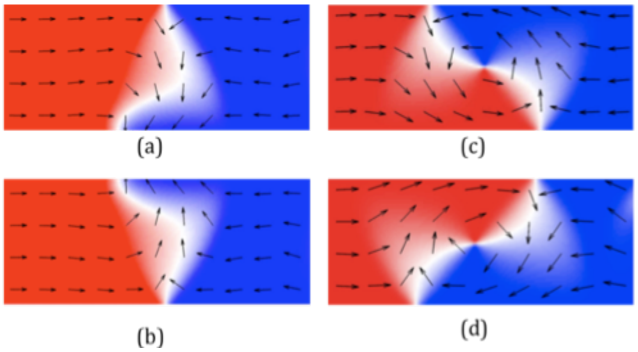

Figure 3: Micromagnetic simulations of domain walls. (a) Transverse wall, with the spins in the wall pointing downwards. (b) Transverse wall with the spins in the wall pointing upwards. (c) Vortex domain wall with a counter-clockwise sense. (d) Clockwise vortex domain wall.

In ChiralMEM the chirality of the domain wall is selectively controlled by the application of a small orthogonal applied field. The physical mechanism for controlling the chirality of the domain wall and selectively pinning the domain wall at notches has been demonstrated both experimentally and through computational micromagnetic simulations [1]. Fig. 2 shows the physical process through micromagnetic simulations. In fig. 2 the chirality of a transverse domain wall is shown to control whether the wall is trapped by a given asymmetric feature. Similar behavior has been shown in simulations and experiments for vortex walls [9, 10]. By selectively controlling the chirality the magnetic field needed to 'pin' a domain wall at an asymmetric feature is significantly different. It is the combination of different asymmetric pinning structures coupled with the different pinning fields that these present to domain walls of different chirality that gives control over the magnetization state obtained and hence the memory state of the cell.

The simplest embodiment of the ChiralMEM multi-bit free layer concept for MRAM is shown in fig. 4. In addition to the conventional two states of opposite magnetization, multi-domain states can be set.

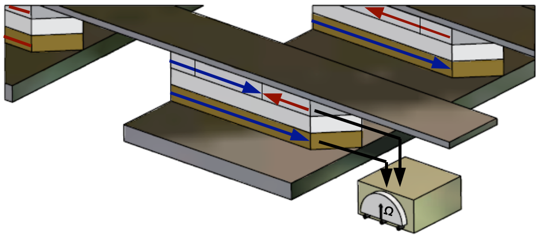

Figure 4: Schematic illustration of a MRAM cell with a ChiralMEM free layer capable of multiple magnetization states control by domain wall chirality selection.

Each of these states in a ChiralMEM layer equates to a different memory value and will have a characteristic readout resistance when incorporated into an MTJ structure, see fig. 5. The ultimate number of bits per cell depends upon the cell geometry, the write-field margin that discriminates between different magnetic states and the readout discrimination. The readout resolution determines the number of different magnetic states that can be distinguished as separate resistance levels of the MTJ structure. For commonly used alumina barrier layers in MTJs, values of the magnetoresistance ratio in excess of 60% [11, 12] are typical and more recently MgO tunnel barriers have shown magnetoresistance ratios of 500% [13]. Fig. 5 shows examples of modeled resistance levels for a six state ChiralMEM cell with reasonable values of magnetoresistance for alumina and MgO barriers respectively.

A further novel concept in the development of ChiralMEM for MRAM applications changes the geometry of the cell structure that offers a more equi-dimensional cell footprint and reduces the 'half-select' write-field problem of conventional MRAM. Fig. 6 schematically illustrates ChiralMEM cells with linear and curved structure. The curved cell consists of a truncated circular MTJ nanostructure that partially encircles a vertical word-line and has a horizontal bit-line crossing the ChiralMEM cell at its nucleation pad.

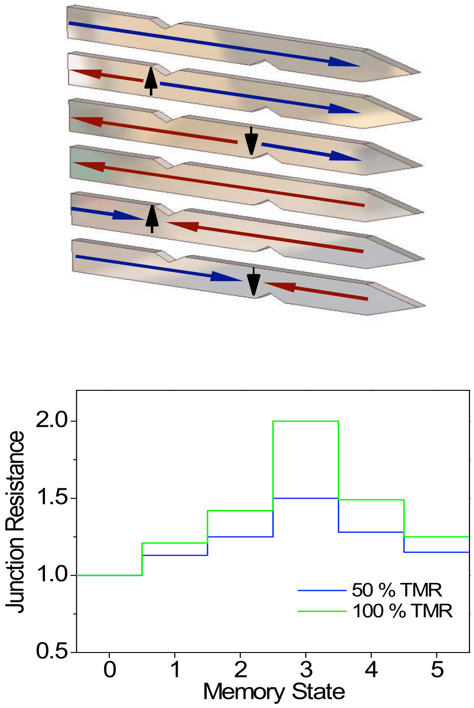

Figure 5: Top, illustration of six different magnetization states (indicated by colored arrows) possible in a ChiralMEM free layer. Lower, calculated resistance steps for an MTJ with six different magnetization configurations in the free layer.

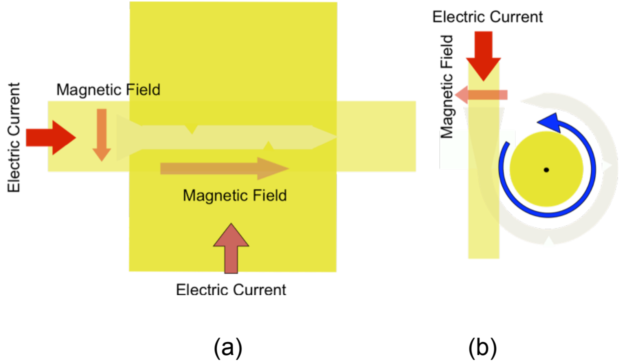

Figure 6: (a) Schematic illustration of simplest embodiment of ChiralMEM structure with word and bit line conductors shown in yellow. (b) Alternative geometry for ChiralMEM with a central word line that is vertical.

Furthermore, this structure allows the potential for significantly increased cell density by stacking of several layers of cells as illustrated schematically in fig. 7. The structure could conceivably increase the number of cells on a given MRAM chip area without significantly increasing total ‘footprint’. The cells are stacked on the vertical word-lines in layers containing bit-lines. The structure has the potential to radically increase the capacity of MRAM bringing them into competition with conventional solid-state memory, although fabrication presents some challenges.

3 SUMMARY

ChiralMEM is a concept for high-density magnetic random access memory that is unique in proposing to create increased data storage density by controlling the formation of multiple magnetic states in each cell. These magnetic states are obtained through the control of a magnetic domain wall based upon the selection of the chirality of the wall structure. The multiple magnetic states equate to multiple memory states in each cell.

To date, micromagnetic simulations and experimental measurements of single layer magnetic nanostructures have demonstrated the physical concept of ChiralMEM for controlling domain wall behavior. Further work is on-going to address the issues of write-field margins, scaling, coupling between the layers in multilayered MTJ structures and the large scale integration into memory devices.

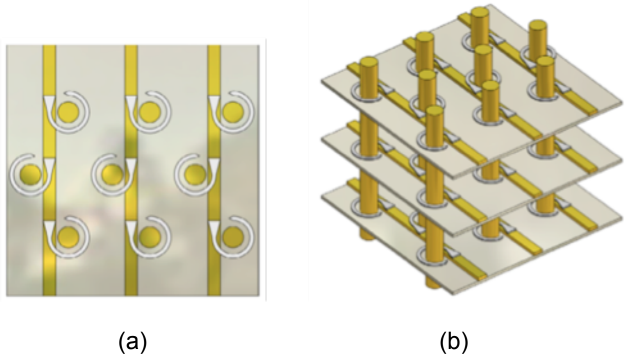

Figure 7: (a) In-plane arrangement of curved ChiralMEM cells forming an array. (b) Concept for stacked arrays of ChiralMEM structures for increased storage density.

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