Design of Multi – Dimensional Variable Capacitors for RF MEMS

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ABSTRACT

In this work, a multi dimensional RF MEMS variable capacitor that utilizes electrostatic actuation is designed. Here we preferred Electrostatic actuation due to its low power consumption. For calculations we assumed 1µm thick silicon monoxide as a dielectric layer for the varactor and a movable membrane is suspended on a 2.5µm thick electroplated gold pedestal. The capacitance between the membrane and the bottom electrode increases as the bias voltage between the membrane and the bottom electrode is increased, eventually causing the membrane to snap down at the actuation voltage. For the varactors designed herein, the actuation voltage is approximately 30 – 90V.The RF MEMS variable capacitor is designed in a CPW topology, with multiple beams (1 to 7) on a single pedestal. For the varactors designed herein, the actuation voltage is approximately 15 – 100V. Full-wave electromagnetic simulations are performed from 1 – 25GHz to accurately predict the frequency response of the varactors. The EM simulations and the measurement results compare favorably. A series RLC equivalent circuit is used to model the varactor and used to extract the parasitic associated with the capacitor by optimizing the model with the measurement results

Keywords: Electrostatic actuation, MEMS, Modeling

I. INTRODUCTION

MICRO-ELECTRO-MECHANICAL- SYSTEM (MEMS) technology offers an attractive capability for RF system. MEMS have enabled the performance, reliability and function of devices to be increased while driving downs their size and cost at the same time. The technology includes circuit tuning elements, resonators, filters, and switches. These low-loss ultra-miniature and highly integrative RF functions can eventually replace classical RF elements and enable a new generation of RF devices. The performance factors, such as low loss and good isolation over a large frequency range, low power consumption etc., make them to use for antenna elements, implementation in phase shifters and RF tuning filters. Since MEMS uses the mechanical movement, so they have relative low switching speed (>8µs).

In this work, we have modeled and simulated a multi dimensional RF MEMS variable capacitor that utilizes electrostatic actuation, and it is preferred over other due to low power consumption. Here the proposed design is based on a CPW topology, with multiple beams supported on a single pedestal. The varactors are modeled using following assumptions:

1. A 1µm thick silicon monoxide (ε_r – 6) is used as a dielectric layer for the varactor.
2. The movable membrane is suspended on a 2.5µm thick electroplated gold pedestal.

Section II includes designing of Capacitor and cantilever, while section III contains results and simulation methodology, and section IV contains conclusion.

II. DESIGN

A multi dimensional RF MEMS variable capacitor with a seven beam topology shown in Fig. 1 is composed of a bottom electrode and movable metallic membranes (beams) on a single pedestal. The beams are movable in a vertical direction normal to the substrate. The gap between the beams and the bottom electrode can be adjusted electrostatically by applying a tuning voltage, resulting in a change in its capacitance. Here we used the coplanar waveguide transmission line as a feed line, with a center conductor width (W) 150µm, the slot width (S) 60µm, ground plane width 800µm, and thru line length of 2000 µm.

The capacitors are designed to have a minimum capacitance value in the up state and a high capacitance value in the down state. The capacitance in the down state can be considered as a metal-insulator-metal capacitor and the value of the capacitance is calculated by the formula given in Eq. 1 [1-3]. This formula is valid to a 1st order approximation as it does not account for the fringing effects.

$$C_{Down} = \frac{\varepsilon_o \varepsilon_r A}{d} \qquad (1)$$

Where ε_o is the electrical permittivity of free space, ε_r is the dielectric constant of silicon monoxide [ε_r – 6], A is the area of the top plate and d is the thickness of the dielectric layer. The capacitance in the up state can be considered as a parallel plate capacitor with two dielectrics

(a) air [ε_{r1} – 1]

(b) silicon monoxide [ε_{r2} – 6] and is calculated using the formula given in Eq. 2

$$C_{Up} = \left[\left[\frac{\varepsilon_o \varepsilon_{r1} A}{d_1}\right]^{-1} + \left[\frac{\varepsilon_o \varepsilon_{r2} A}{d_2}\right]^{-1}\right]^{-1} \qquad (2)$$

Where ε_o is the electrical permittivity of free space, ε_{r1} is the dielectric constant of air, ε_{r2} is the dielectric constant of silicon monoxide [ε_{r2} – 6], A is the area of the top plate and d_1 is the thickness of air and d_2 is the thickness of silicon monoxide layer. The beam area, beam topology, and up/down capacitance for various beam topologies are listed in Table1. The capacitors are designed to have a high capacitance ratio (C_{Down} / C_{Up}) that is typically greater than 14.

Since electrostatic actuation is one of the most popular actuation principles used for RF MEMS applications, there for multiple structures varying in beam size, beam dimension, and the number of beams supported on a single structure are designed. For a simple parallel – plate style capacitor electrostatic actuation is created by applying the voltage across the two plates that are separated by dielectric material. The force generated by applying a voltage can be given by [4-5]

$$F = \frac{V^2 \partial U}{2 \partial d} \quad (3)$$

Where F is the electrostatic force, V is the applying voltage, d is the distance between the two plates, U is the energy stored in the two – plate capacitor, which can be obtained by $CV^2/2$, and C is the capacitance. The beam with higher area would actuate at a lesser applied voltage than the beam with a lesser area. The pull down / actuation voltage (V) is given by [6-7]

$$V = \left(\frac{2}{3}d\right)\sqrt{\frac{2kd}{3\varepsilon_o a}} \quad (4)$$

Where d is the initial beam to electrode distance, ε_o is the electrical permittivity of free space, A is the area of the capacitor and k is the spring constant of the beam which is given by [4-5]

$$k = \left(\frac{32bt^3E}{l^3}\right) \quad (5)$$

Where b is the beam width, l is the beam length, t is the beam thickness and E is the Young's Modulus of the metal used as the beam. From the Eq. 5 it is evident that pull down voltage can vary for a given capacitor area by altering the parameters like length, width and thickness. Considering the physical size of the capacitor and the capacitance value, the above mentioned concept is being used in designing and simulates the varactor which can provide a down state capacitance in the pico farad range. Fig. 1 shows the Momentum simulation setup for a capacitor with a seven beam topology.

In a simplified analysis, the capacitance value rises in steps when various beams snap at their respective pull down voltages. The capacitance at lower voltage values is mainly determined by the up state capacitance (0.35 pF). Beam 1 snaps down at 14.25 volts causing an increase in the capacitance value to 2.45 pF; followed by beams 2 and 3 actuating at 19.20volts to give a combined capacitance value of 3.31 pF; followed by beams 4and 5 actuating at 29.50 volts to give a combined capacitance value of 5.8 pF; Finally beams 6 and 7 actuate at 89.25 volts to give a final capacitance of 15.39 pF as shown in Fig. 2. Practically the capacitance does not increase in steps; the response is more like a smooth slope, with sudden increase in the capacitance value around the pull down voltages for the individual beams. This gradual increase occurs as the beams bend downward with an increase in the actuation voltage, until their respective actuation voltage is met and the beams (ideally) snap down completely.

III. SIMULATION & MODELING

For demonstration purposes, simulated results for the 7-beam topology in various actuation states are shown in Fig. 2 and 3. The input impedance of the EM simulation can be approximated as that of a simple capacitor. The 50Ω feed line used in the EM simulation is 50μm long. Therefore the input impedance is equal to [8]

$$Z_{in} = \frac{1}{j\omega C} \quad (6)$$

A circuit level simulation is performed in ADS with EM simulation data as a data block. The capacitance is extracted from the knowledge of Z_{in}. Rearranging Eq. 6, the capacitance values are extracted by

$$C = \frac{1}{j\omega Z_{in}} \quad (7)$$

Table 3 shows a comparison of the extracted capacitance using Eq. 7 and the calculated capacitance using Eq. 1 and 2. The percentage difference for the extracted capacitance in the down states is less than 8% while in the upstate the percentage difference is approximately 6%.

Equivalent Circuit Modeling

The varactor can be visualized as a series combination of resistance (R), inductance (L) and capacitance (C) to ground. Fig. 5 represents the lumped element equivalent circuit model for the MEMS variable capacitor. The resistance (R) represents the dielectric loss of the capacitor and conductor losses in the metal lines. The resistance is modeled as frequency dependant variable given by Eq. 8 [9]. In Eq. 8, R_{DC} represents the DC resistance of the membrane and B is used to fit the frequency-dependent loss.

$$R = R_{DC} + \left(B\sqrt{f}\right) \quad (8)$$

where, f represents the frequency in Hz. The current crowding and propagation delay in the membrane is modeled as an inductor (L). The capacitance C represents the capacitance of the MEMS variable capacitor that is designed using Eq. 1 and 2. The process of extracting the element values in the model is achieved by using circuit optimization. The inductance L, and the variables R_{DC} and B in Eq. 8 are extracted using optimization. Table 4 compares the extracted capacitance value with the theoretical value. From Table 4, the increase in the up – state capacitance for the extracted value is due to the fringing capacitance and it is close to the calculated value.

IV. CONCLUSION

The MEMS variable capacitor in a CPW topology is designed for multiple beams supported on a single pedestal that utilizes electrostatic actuation principle. Neglecting fringing the theoretical up – state and the down – state capacitance values are calculated using the parallel plate capacitor formula. The theoretical pull down voltage of the varactor is approximately 30 – 90V. A full wave EM simulation is performed from 1 – 25GHz to predict the parasitics associated with the varactor structures. The extracted capacitance from the EM simulations compares favorably with the theoretically used formulae.

V. REFERENCES

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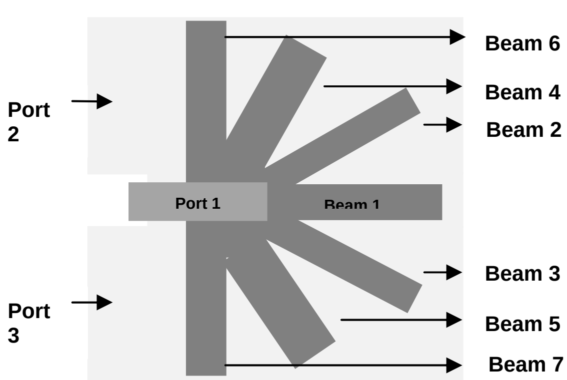

Figure 1: Top View of the 7 – Beam Capacitor Topology used in Momentum Simulation.

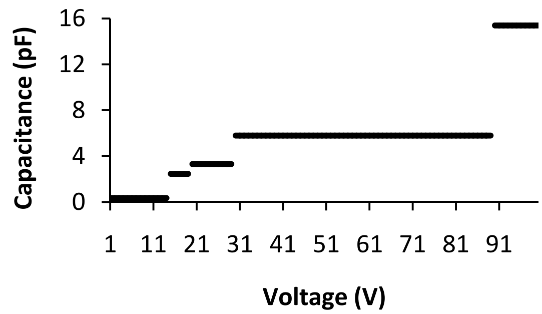

Figure 2: Theoretical Response (I[st] order Approximation) of the Capacitance Value of the Seven Beam Topology.

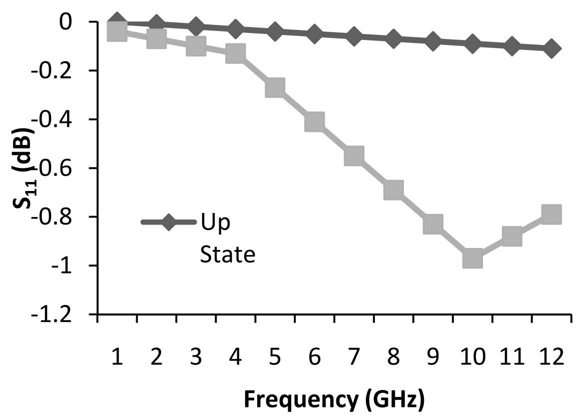

Figure 3: EM Simulation Plots of S_{11} Magnitude as a Function of Frequency for a 7 – Beam Topology at Various Beam States.

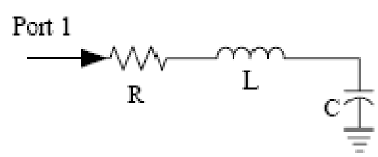

Figure 4: Lumped Element Equivalent Circuit Model for the One – Port MEMS Variable Capacitor.

Beam Topology Structure with 7 Beams	Area of the top plate (µm2) (Calculated)	Up-state capacitance (pF)	Down-state capacitance (pF)
1	2.5×10^5	0.8302	13.268
2	2.6×10^5	0.8634	13.802
3	2.7×10^5	0.8966	14.333
4	2.8×10^5	0.9298	14.863
5	2.9×10^5	0.9630	15.393

Table 1: Physical Characteristics of the Multiple Beam Capacitor Topologies.

	Simulated Actuation Voltage (V)						
	Beam 1	Beam 2	Beam 3	Beam 4	Beam 5	Beam 6	Beam 7
1	14.25	19.20	19.20	29.50	29.50	89.30	89.25
2	13.46	19.20	19.20	29.50	29.50	89.30	89.25
3	14.25	18.47	18.47	29.50	29.50	89.30	89.25
4	14.25	19.20	19.20	28.92	28.92	89.30	89.25
5	14.25	19.20	19.20	29.50	29.50	82.912	85.88

Table.2: Calculated Actuation Voltage for the Beams Incorporated in the Capacitor Structures.

Beam States	Theoretical Capacitance value	EM Simulated Value	% Difference
All beam in up state	0.8966	0.9683	8
All beam in Down state	14.3318	15.1917	6

Table 3: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value.

Capacitance (pF)	Up-State	Down State
Theoretical	0.8966	14.3318
Extracted @ 1GHz	0.9012	14.0312

Table 4: Comparison of the Theoretical Value of the Capacitor (Equation 1 and 2) with the Extracted Capacitance Value in the Up and Down State

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