Memristor Crossbars for Pattern Recognition

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ABSTRACT

A major limitation of conventional microelectronics is the inability to perform pattern recognition at levels comparable with human perception. Software-based solutions of pattern recognition suffer from the delays required for transferring data between a memory and processor while hardware based solutions lack sufficient adaptability to continuously classify new patterns. Recently a new nanoscale circuit element called a memristor was physically realized having both memory storage and signal processing capabilities. The memristor allows data to be stored in multiple resistance states and provides a basis for the creation of circuitry to directly compare binary resistance data to binary voltage data. This paper reviews the state of the art in memristor development and proposes a memristor model and methodology for a pattern recognition circuit design.

Keywords: Memristor, Pattern Recognition, Hysteretic resistance, Crossbar, Nanoelectronics

1 INTRODUCTION

In 1971, Prof. Leon Chua of UC Berkeley published a paper [1] arguing that the conventional view of passive circuitry consisting of resistors, capacitors, and inductors was incomplete. A new fundamental circuit element called the "memristor" (memory resistor) was proposed as a fourth fundamental circuit element based on a relationship between the time integral of voltage and charge. A subsequent paper [2] in 1976 by Chua and Sung-Mo Kang extended and formalized the theory to cover a broader range of systems characterized by a pinched hysteresis curve (Figure 1). Under a sufficiently small voltage the curve demonstrates the linear behavior between current and voltage characteristic of resistors. But as the voltage is increased the slope of the I-V curve switches resulting in a different resistance state. Another characteristic property noted in the 1976 paper was a frequency dependence such that the pinched hysteretic curve degenerates into a linear resistance at high frequencies. However, while the initial papers of Chua and Kang represented a theoretical foundation for the memristor, there was a lack of identification between the theory of memristive systems and a physical implementation to enable integration of memristors in electronic design. This situation changed as of last year when a paper [3] from researchers at HP Labs identified the similarity between the memristor model and the behavior of ionic switching systems formed from metal oxide films with thicknesses on the order of nanometers. A pinched loop hysteretic curve based on Pt-TiO_{2-x}-Pt was found to be identical to that of a memristive system with similar frequency degeneration. But, while HP's group was the first to recognize the connection between the hysteretic property of ionized thin film metal oxides and the memristor theory, they were not the first to identify the hysteretic effects of thin oxides in and of itself. As early as 1967 [4] researchers have identified hysteretic properties of thin film oxides but have lacked a cohesive explanation for the effect. In the past decade this research has accelerated due to the desirability of a new form of higher density non-volatile memory called Resistive Random Access Memory (RRAM) [5, 6].

However, non-volatile memory is not the only proposed application for these devices. With both a theoretical foundation and material examples of memristive materials in place numerous potential applications of memristive systems to self-repairing circuitry [7], analog arithmetic processing [8], signal processing [9], neuromorphic systems [10], and analog control systems [11] have already been proposed. The following sections further detail the memristors as components of crossbar arrays, a circuit model for memristive junctions, and a memristor pattern recognition circuit design approach.

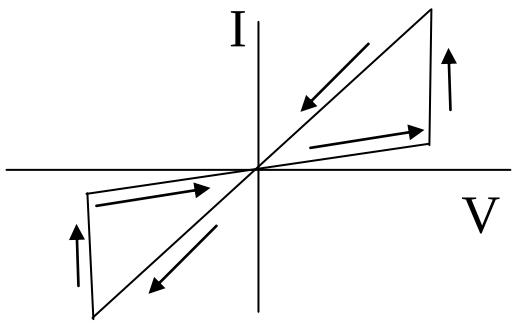

Figure 1: Illustrative example of a typical hysteretic I-V characteristic of thin film oxide memristive

2 MEMRISTOR CROSSBAR DESIGN AND MODELING

Since the late 1990's crossbar arrays (Figure 2a) have been proposed as a candidate platform for future nanoelectronics circuit designs combining high density with reconfigurability [12]. However, depending on the material used in the bistable junction, a noted deficiency in crossbar arrays is internal feedback paths between junctions of the crossbar array [13]. One noted solution to this problem is the fabrication of a pn junction layer (Figure 2b) between the upper and lower wiring [11].

By providing memristors as the bistable junction, a model may be developed for the crossbar transfer function based on Ohm's Law. For an input voltage V_i applied to the i^{th} column wire (with the row wires grounded), the current flow through the memristance material at the intersection of the i^{th} column and j^{th} row is given by :

$$I_{ij} = \frac{(V_i - V_{DIODE})}{M_{ij}} \quad (1)$$

where V_{DIODE} is the diode threshold and M_{ij} is the impedance associated with the memristor. Based on Kirchhoff's Current Law the total current transferred to each row of the crossbar is:

$$I_j = \sum_i I_{ij} = \sum_i \frac{(V_i - V_{DIODE})}{M_{ij}} \quad (2)$$

According to the analysis of [14] the value of the memristance may be approximated at low frequencies by:

$$M_{ij} = R_{OFF}\left[1 - \frac{w(\varphi, v)}{D}\right] + R_{ON}\left[\frac{w(\varphi, v)}{D}\right] \quad (3)$$

$$w(\varphi . v) = \frac{\mu_v}{D}\varphi - \frac{\varepsilon}{\rho D}v \quad (4)$$

where R_{OFF} is the high resistance state, R_{ON} is the low resistance state, $w(\varphi, v)$ is the thickness of the ionized region of the metal oxide, D is the total memristor layer thickness, μ_V is the average ion mobility, ε is the permittivity of the metal oxide, ρ is the ion density, v is the applied voltage and φ is the time integral of voltage. However, experimental pinched hysteresis I-V curves [3,5,13] indicate a region of applied voltage below which ionic transport is not significant and in which the memristance can be approximated as an ordinary resistor having a value of R_{OFF} or R_{ON} according to the previously applied voltages. The ratio of R_{OFF} to R_{ON} has been determined to be as high as 10^6 for some metal oxides [13] leading to an approximation as an ideal switch. The frequency dependent behavior is also indicative of a parallel capacitance (C_p) in which the pinched hysteresis curve degenerates to a singular resistance (R_s) independent of the history of the applied voltage. These combined effects lead to an approximate circuit model for a memristor junction (Figure 3) in which the position of switch S1 is dependent on the voltage states previously applied to the junction.

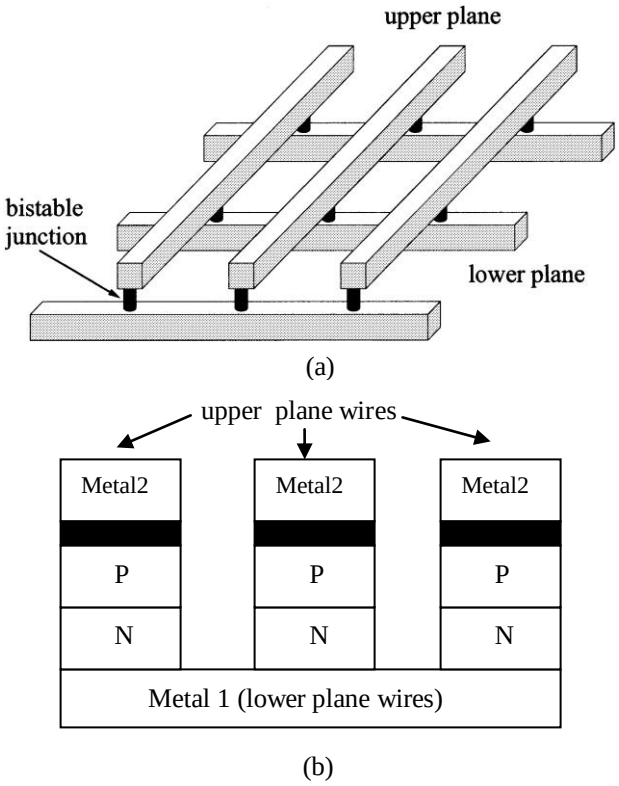

Figure 2: (a) Crossbar array (b) Cross-section of crossbar array incorporating pn junction layer fabricated in series with the bistable junction.

3 PATTERN RECOGNITION CIRCUIT ARCHITECTURE

Some general goals for pattern recognition circuitry are the following:

1. Robustness/invariance to variations of the input pattern.
2. Adaptability of circuit to identify new recurrent patterns.

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3. Speed of responsiveness to pattern inputs.

The first and second of these goals are achievable with software using a sufficiently large memory storing a large number of patterns in a look up table. However, a lag in responsiveness is generated due to time for memory retrieval as the number of stored patterns increases. Application specific electronic hardware can meet the goal of speed of responsiveness but only for a limited number of patterns which sacrifices adaptability. Memristors offer the possibility of a hybrid approach by placing a memristor crossbar array directly in a control signal flow path. The binary resistance states can thus serve both the functions of data storage and signal processing.

One approach to pattern recognition using this capability of memristor crossbars would be to control a current output to be based upon bit matches between input signal states having high or low voltage values and reconfigurable memristance states having high or low resistance values. This may be achieved using a function analogous to XNOR implemented by providing a complementary crossbar array connected to the voltage inputs by inverters. For each crossbar row with a particular row of resistance values a corresponding "inverted" row could then be programmed with the opposite resistance states. Based on Eq. (2) and provided that $R_{OFF}>>R_{ON}$ the current transmitted from each row of the circuit of Fig. 4 would be given by:

$$I_j = \sum_i \frac{(V_i - V_{DIODE})}{M_{ij}(q)} + \sum_i \frac{\overline{(V_i - V_{DIODE})}}{\overline{M_{ij}(q)}} \qquad (5)$$

where the over line notations denote inverted voltage and memristance states. Based on the I-V curves of particular memristive materials, the resistance states associated with the memristances M_{ij} are constant for an applied voltage less than a certain threshold value V_T. Thus the output current from each crossbar junction would be near zero if the voltage logic state is different than the memristive logic state while identical logic states result in a current of approximately V_{HIGH}/R_{ON}. The following table summarizes the possible combinations of voltages and memristance states for a single bit matching combination and provided that $R_{OFF}>>R_{ON}$.

V_i ($<V_T+V_{DIODE}$)	M_{ij}	I_j
$V_{LOW} < V_{DIODE}$ (logic 0)	R_{OFF} (logic 0)	$\approx (V_{HIGH}-V_{DIODE})/R_{ON}$
$V_{LOW} < V_{DIODE}$ (logic 0)	R_{ON} (logic 1)	≈ 0
$V_{HIGH} > V_{DIODE}$ (logic 1)	R_{OFF} (logic 0)	≈ 0
$V_{HIGH} > V_{DIODE}$ (logic 1)	R_{ON} (logic 1)	$\approx (V_{HIGH}-V_{DIODE})/R_{ON}$

TABLE 1 : Binary voltage/memristance comparison states

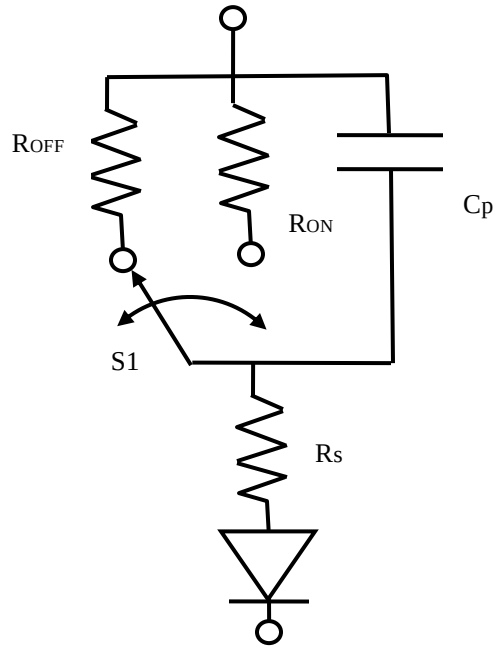

Fig. 3 Approximate small signal circuit model for memristor crossbar junction

For n bit matches between a particular voltage bit patterns and the memristance bit patterns of a particular row the output current is thus:

$$I_j = \frac{n(V_{HIGH} - V_{DIODE})}{R_{ON}} \qquad (6)$$

By setting current level detection circuitry to a threshold in accordance with Eq. 6 bit pattern matching becomes possible. Adjustment of the threshold can provide flexibility in the tolerance for bit errors. In such a case, a digitalized vocal pattern or image including a great deal of corruption could still produce a detection signal which meets the goal of robustness. Since the memristance states in the crossbar array are reconfigurable the goal of adaptability is met. By placing the memristor crossbar array directly in a signal flow path the goal of response speed is met since time required for memory retrieval is eliminated. Thus memristor crossbars offer the possibility of overcoming the limitations of software and hardware in pattern recognition applications.

4 CONCLUSION

This paper has reviewed the characteristics of memristors, provided a basic model characterizing their behavior, and has explained an approach to applications of memristors in pattern recognition having advantages over software and hardware solutions. The binary resistive states

of memristor crossbar junctions essentially function as a reconfigurable bit pattern array which can serve the function of data storage. Memristor crossbar junctions are also capable of acting as resistors within a control signal flow path and set up a decoding transfer function for data processing. Integration of data storage and data processing in a single circuit has the potential to overcome the bottleneck caused by the data retrieval times from increasingly larger memories and provides a route toward the development of electronic architectures having pattern recognition capabilities closer to that of human perception.

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