

Solution-processed ZnO Single Nanoparticle Transistor Using Water-based Dispersions

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ABSTRACT

An integration technique for zinc oxide field-effect transistors processed from nanoparticulate water-based solutions is presented. The devices are single nanoparticle transistors based on drain/source Schottky barriers. Integrated on p-doped silicon standard substrates, the devices showed n-type characteristics and reasonable performance. The threshold voltage, the maximum charge carrier mobility and the current modulation were -0.13 V, 0.05 cm²/Vs and 5×10^3 , respectively, whereas the supply voltage and gate bias were < 5 V at maximum. Because it was expected that nanoparticulate Schottky barrier transistors are subject to some remarkable effects, the conduction mechanisms were examined.

Keywords: ZnO, nanoparticle, Schottky barriers, FET

1 Introduction

Ever since research in the field of organic semiconductors was intensified, interest in alternative inorganic low-cost/low-performance electronics has grown. Among various approaches, e.g. the use of carbon nanotubes or nanowires, the integration of inorganic nanoparticle electronics has become a promising candidate [1–3]. However, many approaches are based on thin-films suffering from poor performance because of interparticulate effects. This disadvantage can be avoided by reducing the active regions to one particle. As a general route for silicon nanoparticle FETs was proposed in [4], the applied integration technique was transferred to ZnO nanoparticles (np-ZnO). A schematic of the proposed transistor device is shown in Fig. 1. The basis of the integration technique is a nanoscaled gap with metal sidewalls representing subsequent drain and source electrodes. A gate dielectric insulates these from the substrate serving as a gate electrode. The application of the nanoparticles is done by a simple spin-coating process of a nanoparticle suspension, whereas the particles self-align in the gaps. Given that gap and particle sizes match, drain and source electrodes are connected by single particles. In principle, the proposed device is a drain/source Schottky barrier transistor, which is superior to a conventional pn-junction MOSFET in terms of short channel effects and process complexity, but also

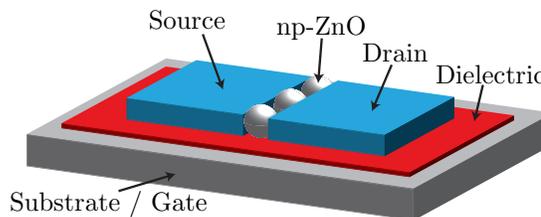


Figure 1: SEM-images of ZnO nanoparticle films deposited from the pure dispersion (top) and the dispersion mixed with the dispersing additive (bottom). The uncovered spot in the upper picture is due to a slight bubble formation during the spin-coating process.

suffers from parasitic effects like increased leakage currents and low current modulations [5,6]. Unlike conventional FETs, much importance has to be attached to the barriers between semiconductor and metal due to performance limiting reasons. Actually, thermal processing of nanoparticulate devices improves the performance. Nevertheless, none of the process steps performed in presence of the applied nanoparticles exceeded 200°C . This maximum temperature is sufficient for the integration of the transistors on most plastic substrates in future.

2 Experimentals

The substrates for transistor integration were standard 4-inch silicon wafers, which were boron-doped and exhibited a specific resistance of $14 \Omega\text{cm}$. After the substrates had been cleaned in a mixture of H_2O_2 and H_2SO_4 at 80°C , rinsed and dried, 60nm silicondioxide were grown thermally. Since the transistors' layout is supposed to be lateral and the active region consists of single particles, metal nanoscaled gaps, which match the particles in size, had to be defined. The gaps were integrated after the technique shown in Fig. 2, which is based on [7] in principle and excels non-optical lithography in cost-efficiency and total process duration. An optical lithography with steep resist edges was done. A conformal layer of low temperature PECVD- SiO_2 was deposited on the resist and etched back anisotropically in order to achieve a spacer at the resist edge, whereas the thickness of the PECVD- SiO_2 determined the later gap size. After the resist was stripped, the spacer re-

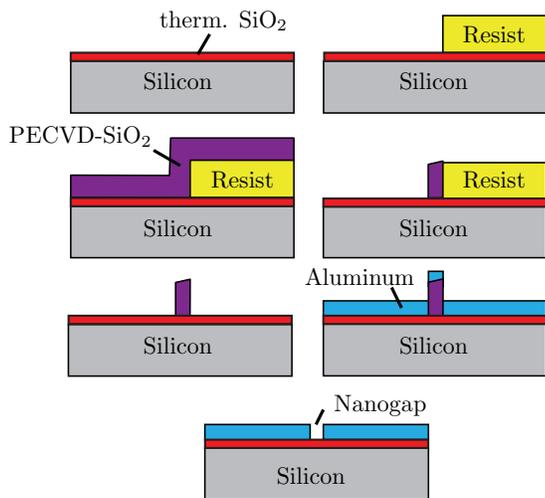


Figure 2: Process flow of the integration of nanoscaled gaps.

remained and a non-conformal layer of aluminum was evaporated. The oxide spacer was removed by reactive ion etching, which was performed under tilted position ($\sim 10^\circ$) to cut the lines and their covering Al off, yielding a nanoscaled gap. The gap size was 100 nm in terms of transistor channel length. This size corresponded to the mean particle diameter.

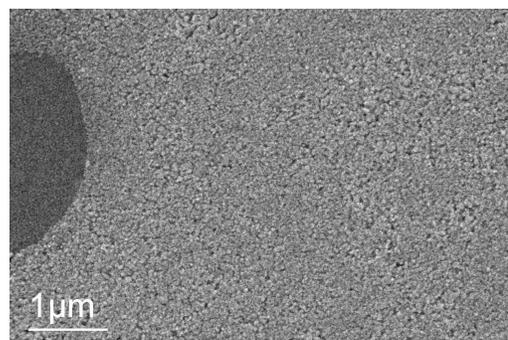
The ZnO nanoparticles were supplied by Evonik Degussa GmbH, Germany. When received, the nanoparticles were already dispersed in water, whereas the manufacturer stated the mass concentration and the mean particle diameter of 35wt% and 100 nm, respectively [8]. No evidence of phase separation could be observed during the complete shelf life of up to 3 months.

Assuming a loose agglomeration of nanoparticles, the suspension was stirred in an ultrasonic bath. Additionally, the influences of two additives (a substrate wetting additive and a dispersing additive) received from Evonik Tego Chemie GmbH were examined. The stabilizers were recommended due to their homogenizing properties [9]. Therefore, one of them was each mixed into the suspension before the ultrasonic bath. Afterwards, the nanoparticles were deposited by spin-coating 1 ml of the dispersion at 2000 rpm for 45 s. In order to evaporate the water, the samples were consecutively baked on a hotplate at 120°C for 2 minutes and in a convection oven at 200°C for 40 minutes.

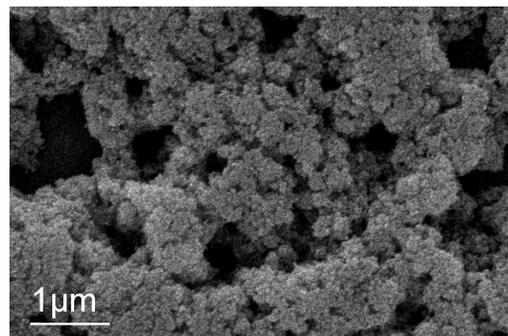
3 Results and Discussion

3.1 Layer Formation

Deposition of the nanoparticles by a spincoating process in the manner specified before resulted in virtually compact films of nanoparticles. Although the proposed device is based on single nanoparticles, the nanoparticle



(a) pure ZnO nanoparticle dispersion



(b) ZnO nanoparticle dispersion with 10 wt% of the dispersing additive

Figure 3: SEM-images of ZnO nanoparticle films deposited from the pure dispersion (top) and the dispersion mixed with the dispersing additive (bottom). The uncovered spot in the upper picture is due to a slight bubble formation during the spin-coating process.

films reveal information on the particle alignment in the nanogaps. Since the particle accumulation in the gaps is self-aligning, the number and position of the nanoparticles is at random. Thus, the particle diameter and the gap size should match each other within a close tolerance. Any deviation would prevent operating transistors.

According to the datasheet, the ZnO nanoparticles are transparent in the visible range of light. Therefore, it was expected to deposit nearly transparent films. Indeed, this expectation was met by the pure dispersion films. However, the films, which were deposited from dispersions containing the additives, exhibited a milky appearance. This opacity indicates a structural modification to larger grain sizes. Apparently, the macroscopic appearance is confirmed in Fig. 3. Whereas films made of the pure dispersion show fine-grained surfaces (Fig. 3(a)), films containing the dispersing additive consist of large agglomerates, which form a fissured surface (Fig. 3(b)). The same holds for dispersion mixed with the substrate wetting additive. Because of the large agglomerates, the np-ZnO does not fit into the nanoscaled gaps. Therefore, both additives seem to be inappropriate for the intended purpose.

3.2 Electrical Characterization

The on-wafer electrical characterization of the integrated devices was performed using a HP4156A semiconductor parameter analyzer. As expected, measurements of devices with nanoparticles, which were laced with additives, did not reveal any reasonable data. The use of pure dispersion, however, led to transistors functioning properly. Fig. 4 shows the transfer characteristics of a typical device, which apparently operated in n-type mode. The I-V-trace can be modeled by the basic equations for field-effect transistors:

$$I_D = \beta \frac{W}{L} \left[(V_{GS} - V_t) - \frac{V_{DS}}{2} \right] V_{DS} \quad (1)$$

in the linear regime and

$$I_D = \frac{\beta W}{2 L} (V_{GS} - V_t)^2 \quad (2)$$

in the saturation regime.

Analysis of the transfer characteristics revealed a threshold voltage and an ON/OFF-current ratio of $V_t = -0.13$ V and $> 10^3$, respectively. The threshold voltages of all measured devices were within a range from -0.5 V to 0 V, clearly indicating depletion type transistors. Furthermore, the maximum effective charge carrier mobility was $0.05 \text{ cm}^2/\text{Vs}$, which is one of the highest values reported for ZnO nanoparticle transistors. In contrast to ZnO thin-film transistors, the demonstrated single np-ZnO transistors operated at low supply voltages (< 5 V) due to a considerably reduced number of interparticulate interfaces and definite short current paths [9]. In reverse mode, the drain current is relatively high as expected from Schottky barrier transistors. In the same way, the Schottky barriers at drain and source interfaces affect the contact resistances adversely. Thus, only slight slopes in the low- V_{DS} -portion of the output characteristics (Fig. 5) occur.

A degradation effect was observable, while transistors were under operation. This degradation of ZnO transistors has already been described in [10] and is caused by saturation of trap states. Comparing Fig. 4 and Fig. 5, it is evident, that the maximum current of the transfer characteristics is inferior to the current of the output curves by a factor of 10, because their measurement were done one after the other with a 15 minutes delay. In order to understand the conduction processes dependent on the gate bias, two I-V-traces were picked out of the output characteristics of an arbitrary device (Fig. 6). The first curve in the lower part of the diagram represents the approximate off-state current of the transistor at $V_{GS} = 0$ V, whereas the upper curve is the on-state current at $V_{GS} = 4$ V. Dividing the curves into sections and fitting the traces after assumed physical conduction models leads to four and three distinct sections in the cases of the off-state and on-state current, respectively.

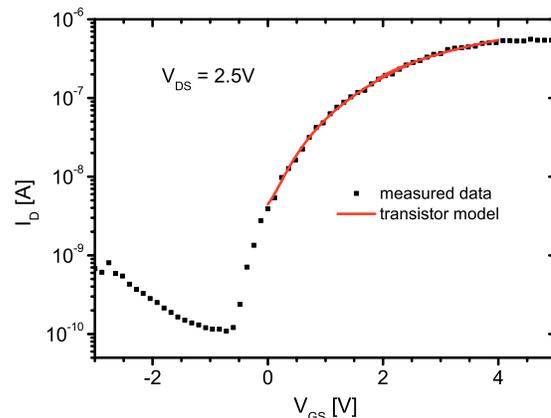


Figure 4: Semilog-plot of the measured transfer characteristics of a typical np-ZnO transistor (black rectangles). The I-V-trace was modeled after (1) and (2) (red line). The geometrical transistor width was $100 \mu\text{m}$.

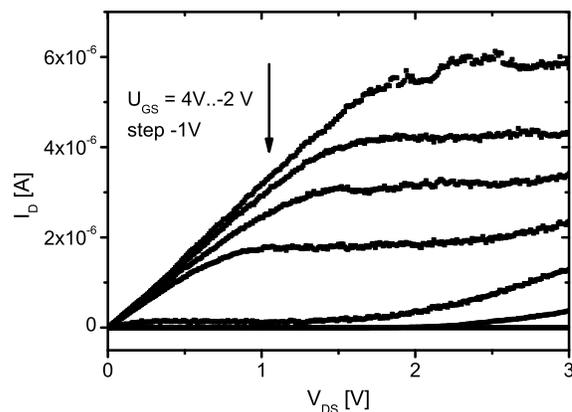


Figure 5: Plot of the measured output characteristics of a typical np-ZnO transistor (same as in Fig. 4)

The off-state current is mainly dominated by barrier- and trap-limited effects, which is reasonable due to pronounced barriers and defect-states in the particles. The conduction mechanism is influenced by the increasing drain voltage, which provides improvement rather of the semiconductor's conductivity than of the barriers. For medium V_{DS} an exponential increase of the current was identifiable. Its close relation to non-ohmic contacts at either the drain or the source electrode is self-evident. At an higher gate bias (upper trace), a section dominated by ohmic conduction occurs. This indicates a shift of the Quasi-Fermi level causing a high free charge carrier density. That is why charge carriers can easily drift from one electrode towards the other. Actually, a tunneling effect was not observable. Therefore it can be assumed, that the relevant contact barriers has

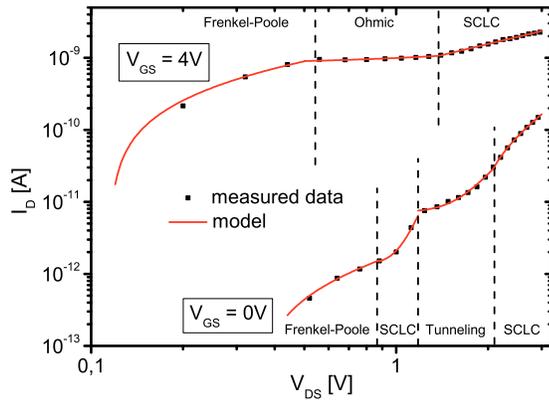


Figure 6: Loglog-plot of two selected I-V-traces of the output characteristics with $V_{GS} = 0\text{ V}$ (lower curve) and $V_{GS} = 4\text{ V}$ (upper curve). The measured data are marked by rectangles, the modeled curves are represented by the red lines.

narrowed so far, that they provide quasi-ohmic behavior. In both cases the currents were space-charge-limited (SCLC) in the high V_{DS} -portion. Obviously, the influence of all contact barriers can be neglected, so that charge injection was performed sufficiently.

4 Conclusion

A solution-processed ZnO single nanoparticle transistor was demonstrated. The highest temperature in presence of the semiconductor was 200°C . Although the process refrained from annealing at higher temperatures, the devices exhibited properties comparable to high temperature annealed ZnO thin-film transistors, which have to be operated at much higher voltages. Therefore, the presented transistors revealed one of the best performances of low-temperature processed ZnO transistors reported to date. The conduction processes were examined, whereas a significant change of the conduction modes was observed.

Further work on the exchange of the gate dielectric by polymer materials would qualify the devices for integration on flexible substrates featuring reduced manufacturing costs.

5 Acknowledgement

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