Improved layout dependent modeling of the base resistance in advanced HBTs

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Abstract - A physics-based analytical set of equations is applied to calculate the internal and external base resistance of SiGe HBTs for a practically relevant variety of single base contact (SBC) layouts. Through comparison with results from quasi-3D device simulations the accuracy of the equations is verified and validity limits are determined. Additionally, the impact of a broken silicide layer on the base resistance is investigated.

1. INTRODUCTION

High-speed wireline and wireless communication circuits and systems are increasingly realized using Silicon-Germanium (SiGe) HBTs since their performance has benefited tremendously from integration into CMOS processes. One of the most important parameters of HBTs having significant impact on speed and noise behavior is the base resistance r_B. Therefore, accurate analytical equations are required for describing r_B as a function of bias, temperature, and layout. The goal of this paper is to provide insight into layout (i.e. geometry) dependence of the base resistance r_B and the associated current flow in structures with base contact schemes that have become increasingly common in advanced HBTs.

In [1,2] a set of equations was presented which has been widely used for calculating the layout dependence of the base resistance for circuit optimization and statistical design (e.g. [3,4,5,6]). However, bipolar process technology has changed significant since [1,2] were published. Modern SiGe HBT structures have a silicided external base region, which makes single-base contact schemes feasible. In some cases [7], the base is even contacted at the emitter foreside in order to reduce the BC capacitance and the collector resistance. Also, the ratio of the base link sheet resistance r_{Sl} to the internal base sheet resistance r_{SBi} in HBTs, $r_{Sl}/r_{SBi} \approx 1$, is significantly larger than in the BJT processes ($r_{Sl}/r_{SBi} \approx 0.2$) considered in [1,2]. Furthermore, shrinking vertical and lateral dimensions occasionally cause the silicide to break. Although this is a reliability issue that needs to be eliminated in a production process, it is useful to at least obtain a feeling for its impact on r_B.

The applicability of the equations in [1,2] has been evaluated for the above mentioned structures. The observed errors for some cases led to a more comprehensive improved (for double- and single-base contact structures) and extended (for foreside-base structures) set of compact equations [8]. In this paper, well-proven quasi-3D device simulation is employed for investigating a variety of base contact arrangements and layout dimensions. An npn transistor structure in forward d.c. operation is assumed. The term "low-bias" is synonymous with "negligible emitter current crowding". Hence, the internal base sheet resistance already assumes its operating point dependent value at low-bias which can be different from its zero-bias value.

2. METHOD

As shown in [1] the flow lines associated with the base current can be transformed into a 2D plane as shown in Fig. 1. The various base current contributions supporting the current flowing into the internal base are indicated by I_{front}, I_{fore}, I_{back}. The sum of these currents is injected across the BE junction. The treatment of general emitter geometries is based on the hole transport and continuity equation.

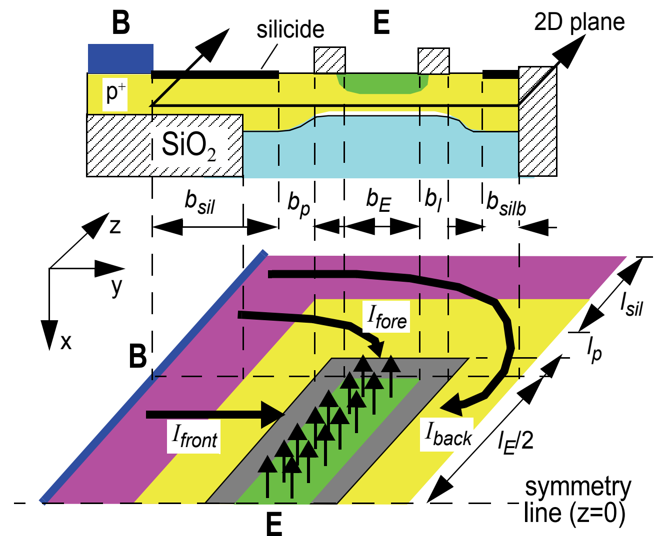

Fig. 1 Schematic cross-section of a single-base structure (with slot contact) and projection of the base current flow path into a 2D plane. The long arrows in the yz-plane indicate the relevant current contributions to the front, fore and back side, while the short arrows pointing out of the internal base region (in -x-direction) represent the base current injected into the emitter.

The quasi-3D simulation method is based on the reasonable assumption that the hole quasi-fermi potential φ_p does not depend on the vertical dimension x over the interval where the hole density significantly contributes to the sheet resistance of a particular region. Then the sheet resistance in the resulting 2D simulation structure can be written as

$$r_S = (q\bar{\mu}_p \bar{N} L_x)^{-1} \tag{1}$$

with L_x as unit dimension in x-direction. In the simulation, the desired sheet resistance value is adjusted by the average mobility value $\bar{\mu}_p$ rather than through the average doping concentration $\bar{N}$ in order to avoid non-physical abrupt

energy barriers between the regions. The bias dependence of the internal base sheet resistance r_{SBi} is not included in the simulation (although possible) since the focus is on the geometry dependence of r_B and since its bias dependence is weak for SiGe HBTs.

The base resistance is obtained using eq. (1) in [1]. Compared to the Fourier series solution in, e.g., [9] this approach permits more general and realistic structures as well as an investigation of the high-frequency small-signal behavior.

3. INVESTIGATED STRUCTURES

The layout sketched in Fig. 1 with a single parallel base contact (SBC) were investigated with different dimensions. The corresponding values for the structures presented in this paper are listed in Table 1. In all cases the emitter width is $b_E = 0.25\mu m$. Each structure contains the following regions:

- A silicided region with sheet resistance r_{Ssil} and the dimension b_{sil} at the frontside, l_{sil} at the foreside, and b_{silb} at the backside (SBC structure only); both r_{Ssil} (= 8, 16)Ω/sq as well as l_{sil} and b_{silb} were varied.
- A poly-silicon on mono-silicon region with sheet resistance $r_{Sp} = 25\Omega/sq$ and dimension b_p at the frontside as well as l_p at the foreside. This region is missing in those processes where the silicide is defined by the BE spacer.
- A link region surrounding the emitter with sheet resistance $r_{Sl} = 2200\Omega/sq$ and width b_l.
- An internal base region (under the emitter) with the sheet resistance $r_{SBi} = 2200\Omega/sq$ and dimensions b_E and l_E.

value/μm↓	b_l	$b_p = l_p$	b_{sil}	l_{sil}	b_{silb}	r_{Ssil}
case 1	0.15	0.15	0.2	0.2	0.2	8
case 2	0.15	0.15	0.1	0.1	0.1	8
case 3	0.15	0.15	0.1	0.1	0.1	16

Table 1: Dimensions (in μm) used for the simulated structure. Note that the ratio of the dimensions is important rather than their absolute values; r_{Ssil} values in Ω/sq.

4. SINGLE-BASE CONTACT STRUCTURES

Single-base contact structures are often favored in applications due to the reduced base-collector capacitance and collector resistance. The schematic layout of the simulated structures is shown in Fig. 2 along with the partitioning of the various regions for resistance calculations and with the resulting resistance network. Every node in the equivalent circuit corresponds to an equipotential line in the structure. In order to be able to separate the description of the bias dependent internal base resistance r_{Bi} from the bias independent external base resistance r_{Bx}, the boundary between base link and internal transistor (underneath the emitter) is assumed to be an equipotential line. As can be seen in Fig. 3 this is (still) a fairly good assumption for a structure with an aspect ratio $b_E/l_E = 1/5$, but begins to fail on the backside for longer stripes [8] or higher silicide resistance. The deviation at the corners due to the rounding of the lines will even disappear in fabricated structures due to lithography reasons.

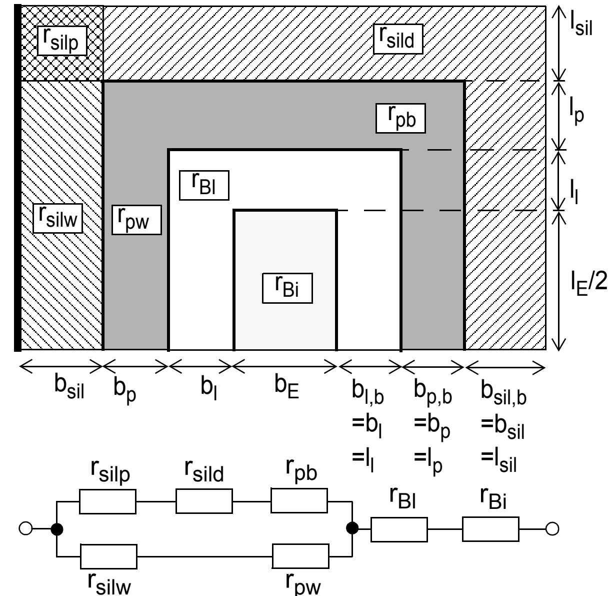

Fig. 2 The various resistance components within the SBC structure and the associated equivalent circuit. The thick lines indicate the assumed equipotential lines.

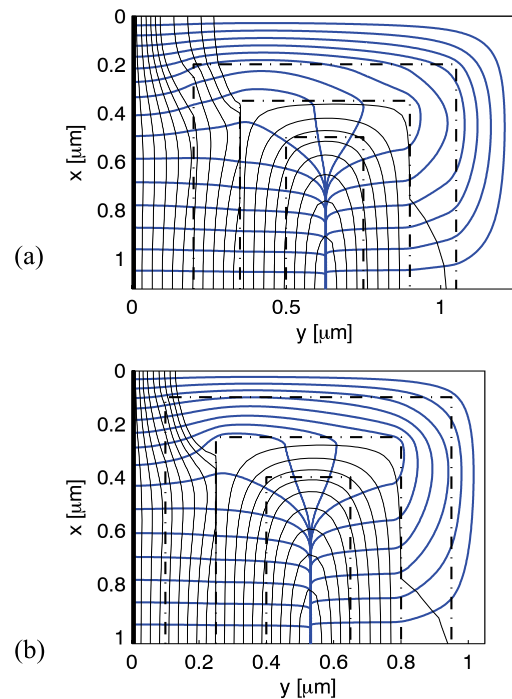

Fig. 3 Current flow and equipotential lines in an SBC structure for the emitter aspect ratio $b_E/l_E = 0.25/1.25$: (a) standard silicide widths (case 1), (b) reduced silicide widths (case 2).

In contrast to BJT processes the base layer epitaxy leads to a link sheet resistance r_{Sl} that is very close to the internal base sheet resistance r_{SBi}. As a consequence, the link resistance r_{Bl} has become the dominant contribution to r_{Bx} and is, besides the silicidation, the main reason why single-base contact structures have become so popular in applications. This has increased the importance for an accurate description of the layout dependence of r_{Bl}. According to Fig. 3, the equipotential lines at the emitter corners look rather like quarter circles, which will be true even more in realistic structures with corner rounding. Assuming an emitter window rounding radius b_{Er} the corner link resistance r_{lc} is given by the expression obtained for a cylindrical resistance structure (e.g. [11])

$$r_{lc,\ln} = \frac{r_{Sl}}{2\pi}\ln\left(1+\frac{b_l}{b_{Er}}\right) \quad \text{for} \quad b_{Er} \le \frac{b_E}{2}. \tag{2}$$

This resistance is the dominant component of r_{Bx} in a square or short structure. A sufficiently accurate approximation without the ln() term can be obtained by assuming an average radius of (b_{Er}+b_l/2),

$$r_{lc} \cong \frac{r_{Sl}}{2\pi}\frac{b_l}{(b_{Er}+b_l/2)} \quad \text{for} \quad b_{Er} \le \frac{b_E}{2}, \tag{3}$$

with $b_{Er} = b_E/2$ for $b_{Er} > b_E/2$. The latter approximation deviates less than 5% from eq. (2) for the chosen b_{Er}=0.125µm (cf. Fig 4).

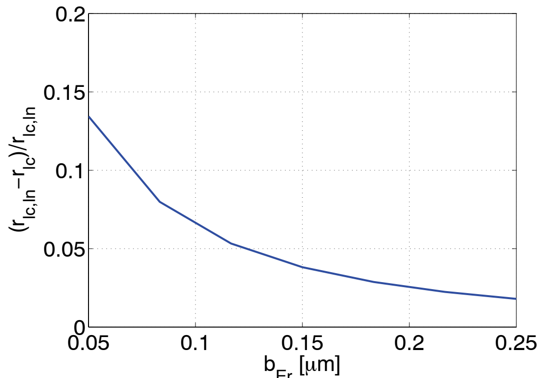

Fig. 4 Relative deviation of the corner resistance value using (3) with the layout dimensions of Table 1.

In the remaining link region at the front, foreside and backside a fairly parallel current flow is observed, allowing the corresponding resistance to be modeled as

$$r_{lw} = \frac{r_{Sl}}{2}\frac{b_l}{l_E+b_E-4b_{Er}} \quad \text{for} \quad l_E \ge b_E \ge 2b_{Er}. \tag{4}$$

The total link resistance is then given by the parallel circuit of the above two components:

$$r_{Bl} = (1/r_{lc}+1/r_{lw})^{-1}. \tag{5}$$

If the dimensions of the external base are reduced, the distributed resistance r_{sild} around the emitter length becomes more important since this region supports the backside of the internal transistor.

The distributed current flow in this region can be considered to consist of two components as sketched in Fig. 5. According to [10] the equivalent resistance for the region y=[1.5a,1.5a+l] can be written

$$R_{eq}(\delta) = r_S\sqrt{\frac{\delta}{1-\delta}}\coth\left[\frac{l}{a\sqrt{\delta(1-\delta)}}\right]. \tag{6}$$

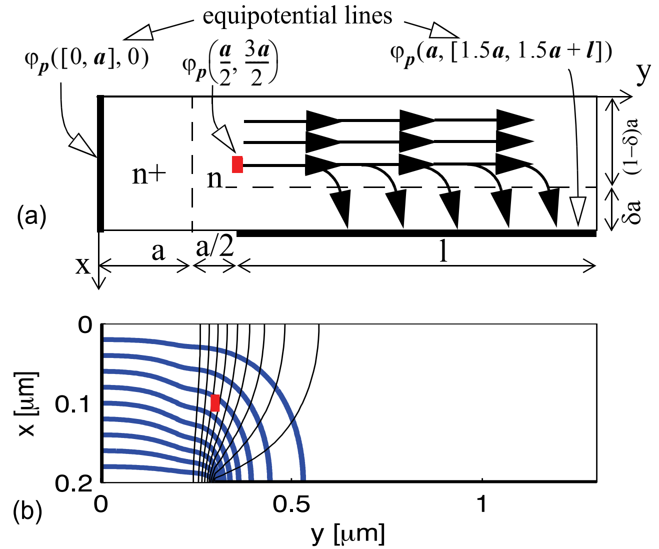

Fig. 5 (a) Schematic simulated test structure for determining the partitioning factor in the distributed resistance calculation, and (b) resulting current flow from the left contact to the lower contact and equipotential lines for l=5a and r_S=8Ω/sq.

To determine δ two different methods for calculating R_{eq} from device simulation have been used. Using a reference quasi-fermipotential and the simulated current I follows

$$R_{eq1} = \frac{\varphi_p\left(\frac{a}{2},\frac{3a}{2}\right)}{I}. \tag{7}$$

According to Fig 5b, assuming an equipotential line in x-direction at y=3a/2 is only an approximation. Thus, an average voltage drop between y=0 and 3a/2 is used to correct the total resistance

$$R_{eq2} = \frac{\varphi_p(0,0)}{I} - \frac{1}{a}\int_{y=0}^{1.5a} r_S(y)dy \tag{8}$$

using the sheet resistance r_S(y) of this area.

The obtained resistance range enclosed by the values of the two applied methods as shown in Fig. 6 confirms the value $\delta = 0.15$ used in [1,2]. This also holds for different sheet resistances.

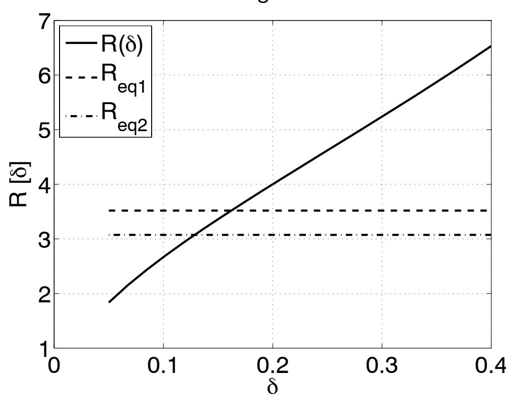

Fig. 6 Distributed resistance respective to the chosen δ (solid) and the results of the two methods for the resistance determination (dash, dash-dot) for r_S=8Ω/sq.

As observed in Fig. 3, a complete separation between silicide and poly-silicon region is not possible. Following the approach in [2] and sketched in Fig. 2, the front region and the remaining fore and back region are modeled separately as parallel current paths. An improved version of the corresponding analytic equations is presented in [8].

For long emitters the current flow into the link and internal base region decreases on the backside. In how far this impacts the internal base resistance is shown in Fig. 7. Here the improved transition function f_i that was originally introduced in [2] is shown versus an also improved transition variable given by the parallel connection of the silicide and poly-Si resistance,

$$u = \frac{\left(\frac{b_{sil,b}}{r_{Ssil}(d_p + 2l_p + b_{sil,b})} + \frac{b_p}{r_{Sp}\,d_p}\right)^{-1}}{r_{SBi}(b_E/l_E)}, \qquad (9)$$

with $d_p = 3b_l + b_E + l_p + l_E/2$ as average fore and back side current path in the poly-silicon layer. The denominator is just a normalization variable. For short emitters or sufficiently low-ohmic silicide regions (i.e. small u) the current flow is similar to that of a double-base contact structure, and so is the resistance. However, for long emitters or relatively high-ohmic (e.g. narrow) silicide regions (large u) r_{Bi} tends to approach the value of a single-base *walled* structure, which is a factor 4 larger than for a double-base structure.

Table 2 contains a comparison of the simulated and modeled resistance values for selected structures using physics-based equations of [1,2,8]. Good agreement is obtained for almost all layout variations. Even for the most critical layouts with narrow silicide width, high silicide resistance and very low b_E/l_E ratios the deviation is below 10%.

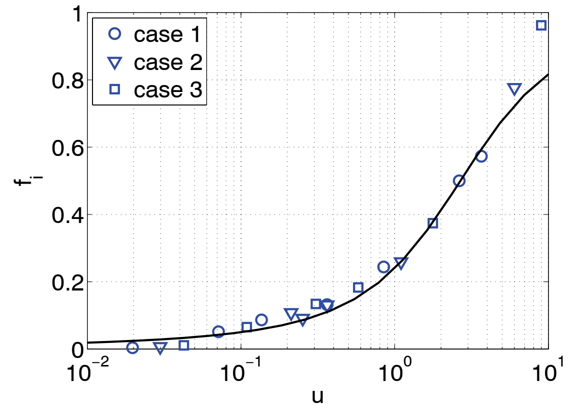

Fig. 7 Transition function f_i vs. transition variable u for all investigated SBC structures. Simulation is indicated by symbols. The solid line represents the analytical equation given in [8].

b_E/l_E r_B/Ω	1/1	1/5	1/10	1/20	1/40
case 1: sim	346	146	83.4	47.6	28.8
model	358	142	81.6	47.1	28.6
case 2: sim	348	148	86.1	50.7	31.6
model	360	143	83.9	50.1	30.1
case 3: sim	351	152	89.8	54.3	34.2
model	364	146	87.1	53.3	31.2

Table 2: Total base resistance values for the SBC structure: comparison between device simulation and compact model.

5. FORESIDE-BASE CONTACT STRUCTURES

Placing the base contact at the emitter foreside as shown in Fig. 8 can further reduce the base-collector capacitance and collector resistance. This may come though at the expense of limitation in emitter length due to a significantly increased base resistance if external dimensions continue to shrink and the silicide sheet resistance keeps increasing. The used dimensions and silicide sheet resistance values are listed in Table 1. Fig. 8 also exhibits the intended equivalent circuit which is based again on equipotential line considerations. Since the existing compact equations in [1,2] do not cover this case at all, a new set of equations was developed in [8] with f_i for modeling r_{Bi}.

As shown in Fig. 9(a), for a wider and low-ohmic silicide region the current flow lines in the poly-silicon and link region are almost perpendicular to those in the silicide region, indicating that these regions are more or less entirely supported by the silicide region. If the cross-section of the latter is reduced and the sheet resistance increased, the poly-silicon region starts to take over more of this current and a

simple compact description based on perpendicular current flow in the poly region becomes less accurate for ratios $b_E/l_E < 0.2$. As long as $r_{Sp} << r_{Sl}$ though, (6) can then be applied to the poly region as in [1,2]. Generally, an accurate compact solution is more complicated than for SBC structures.

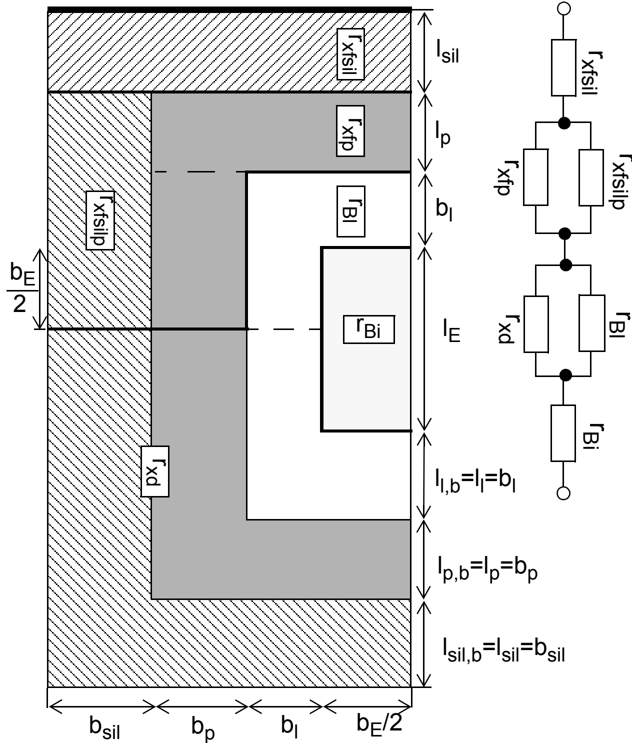

Fig. 8 The various resistance components within the FBC structure and the associated equivalent circuit. The thick lines indicate the assumed equipotential lines. For fabrication reasons, generally $l_p = b_p$.

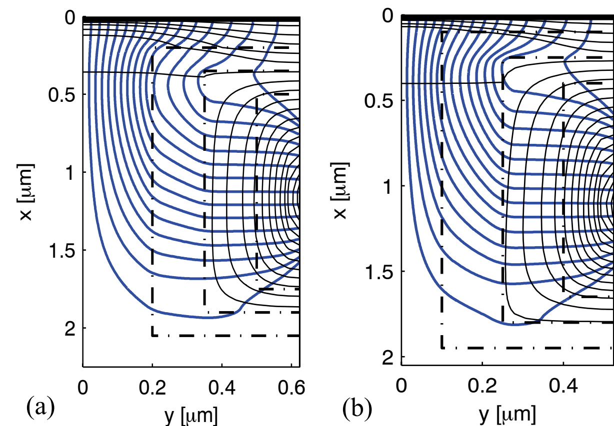

Fig. 9 Current flow and equipotential lines in an FBC structure with n_B=1 for the emitter aspect ratio $b_E/l_E = 0.25/1.25$: (a) standard silicide widths $l_{sil}=b_{sil}=0.2\mu m$, (b) reduced silicide widths $l_{sil}=b_{sil}=0.1\mu m$ and $r_{Ssil}=16\Omega$/sq.

As the results in Table 3 show the model equations give good results down to a b_E/l_E ratio of 0.2. For smaller b_E/l_E ratios the simulated values drop faster than the modeled ones. However, both show the same trend for even larger b_E/l_E ratios at which the base resistance starts to increase again. This caused by the simultaneous increase of the silicide resistance and decrease of the internal and link resistance with l_E; i.e. their ratio is proportional l_E^2.

b_E/l_E / r_B/Ω	1/1	1/5	1/10	1/20	1/40
case 1: sim	346	146	79.6	73.5	75
model	358	142	119	126	127
case 2: sim	348	148	86.5	72.4	106
model	360	143	127	125	146
case 3: sim	351	167	83	91	144
model	364	153	122	140	165

Table 3: Total base resistance values for the FBC structure: comparison between the results of device simulation and compact model.

6. BROKEN SILICIDE

Shrinking dimensions of the silicide region can lead to a "broken" layer disconnecting the remaining portion of the structure from the contact. In order to provide a feeling for the difference in base resistance, the SBC and FBC structures were simulated for case 2 with two different locations of the interruption. The latter forces the flow lines through the higher-ohmic poly-silicon layer, which is shown for the SBC structure in Fig. 10 and for the FBC structure in Fig 11.

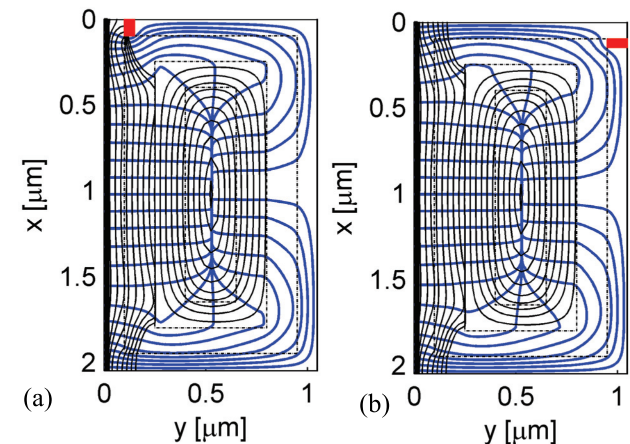

Fig. 10 Current flow and equipotential lines in an SBC structure with different locations of broken silicide layer: (a) "open" at foreside (r_B=148.5Ω), (b) "open" at backside (r_B=148.07Ω). Emitter aspect ratio $b_E/l_E = 0.25/1.25$, $l_{sil}=b_{sil}=0.1\mu m$, $r_{Ssil} = 8\Omega$/sq.

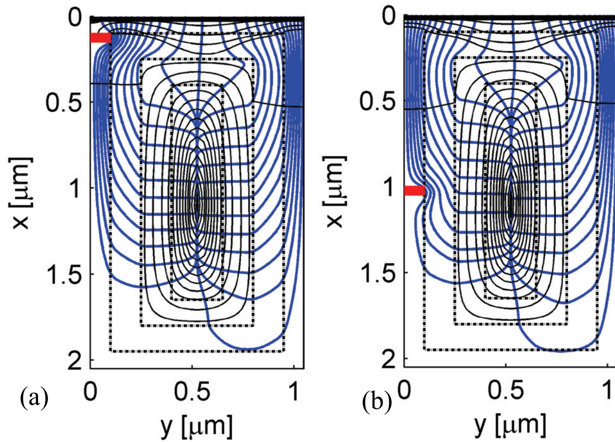

Fig. 11 Current flow and equipotential lines in an FBC structure with different locations of broken silicide layer: (a) one-sided "open" at foreside y = 0 (r_B=159.73Ω), (b) one-sided "open" at $y = l_E/2$ (r_B=158.88Ω). Emitter aspect ratio b_E/l_E = 0.25/1.25, l_{sil}=b_{sil}=0.1μm, r_{Ssil} = 8Ω/sq.

Although the impact of the interruption of the silicide on the current flow lines is clearly visible for the respective two different cases, the results show negligible differences in the total base resistance. This is mostly due to its much lower value compared to that of r_{SI} and r_{SBi} as well as due to the relatively high aspect ratio (b_E/l_E = 0.2).

7. CONCLUSIONS

Improved physics-based compact analytical formulations presented in [1,2,8] for modeling of the base resistance of SiGe HBTs have been applied to:

- single-base contact in parallel to the emitter;
- base contact *perpendicular* to the emitter finger;
- variations in the external base layout dimensions;
- a large emitter aspect ratio range.

The equation set has been compared to the solution of quasi-3D device simulation. An accurate description of the investigated parallel single base contact structures for a large variety of geometries has been demonstrated. For the foreside contact arrangement the equations are accurate down to an emitter aspect ration b_E/l_E of 0.2. For smaller values they still show the same trend though indicating the fundamental effect is included in the equations.

Simplified formulations for the corner component of the base link resistance and the distributed silicide resistance have been validated.

Finally, the impact of a broken silicide layer on the total base resistance was shown to be negligible at least for emitter aspect ratios down to 0.2. This alleviates process reliability issues.

8. ACKNOWLEDGMENTS

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