

Model Implementation for Accurate Variation Estimation of Analog Parameters in Advanced SOI Technologies

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ABSTRACT

Analog design uses transistors with longer channel length for high performance. Transconductance (g_m), Output Resistance (R_{out}) and Intrinsic Gain ($g_m \times R_{out}$) form the metric to gauge this performance. It is critical to design these circuits for manufacturing variability. This work presents a systematic compact modeling approach to capture analog variation in compact models. We show that the variation in R_{out} is very well correlated to the variation in DIBL, especially if the transistors are biased at around 100-200mV gate-overdrive. We observe that this correlation becomes stronger as the channel length increases. We propose a sub-circuit based approach to model DIBL variation in the corner models. This method provides accurate variability estimates of g_m and R_{out} in the compact models for 65nm and 45nm technologies.

1 INTRODUCTION

Device design in advanced microprocessors is driven by the need of high I_{on}/I_{off} ratio since the majority of the chip deals with digital operation involving logic levels 0 and 1. Channel length scaling along-with appropriate T_{ox} , doping density and junction depth scaling is done to achieve higher drive current at a given leakage level for these logic circuits. The device requirements are often conflicting between digital and analog circuits [1]. For analog circuits, high g_m , R_{out} and intrinsic gain ($g_m \times R_{out}$) are important DC parameters. g_m increases and R_{out} decreases with increasing channel length [2]. However, the degradation in R_{out} is severe than the increase in g_m so intrinsic gain decreases with reduction in the channel length (add figure here from that data). Also, R_{out} for the floating body (FB) PDSOI transistors is lower than the body-tied (BT) transistor due to kink and capacitive coupling [1]. Therefore, long channel BT transistors are used in the analog circuitry in a microprocessor.

Normally, the circuits are designed to tolerate manufacturing variability for high yield. Usually, different process corners are provided in the compact models for the designers to design for robustness. In general, these corners

are very useful for estimating parameters like drive current, threshold voltage etc. There hasn't been much work done to understand the sources of variation for analog parameters such as g_m , R_{out} and their model-to-silicon correlation. This paper is divided into two sections. The first section focuses on the observations based on the data. The assessment of current variation models, their deficiency and new methodology for better accuracy are discussed in the second section.

2 DEVICE CHARACTERIZATION

DC device parametric has been characterized for analog specific BT transistors in AMD technology, described by Horstmann et. al. [3]. The sample space is big enough for accurate statistical conclusions. g_m and R_{out} are measured at gate-overdrive of 100mV, 200mV and drain bias of $0.5V_{dd}$.

3 RESULTS & DISCUSSION

3.1 Data Analysis

Throughout this paper, the variation in the data is defined as the ratio of 1 sigma deviation of the distribution to its median. Fig. 1 shows the variation of g_m , R_{out} for 65nm and 45nm technologies. Suffix 1 and 2 represent parameters measured at a fixed drain bias and 100mV, 200mV gate-overdrives respectively. R_{out} is a strong function of channel length [2]. Therefore, it is intuitive to expect R_{out} variation to reduce from shorter to longer channel lengths. However, as shown in Fig. 1, the R_{out} variation behaves non-monotonically with the channel length. This is due to halo doping in a MOSFET. For halo-based processes, R_{out} for long channel devices is determined by DITS [5], [6]. This is evident from Fig.2 which shows normalized R_{out} as a function of normalized DIBL. Channel length increases from L1 to L5. It can be seen that the impact of DIBL variation on R_{out} is the strongest for the longest channel length.

From Fig. 1, it can also be inferred that the effect of DITS variation is reduced as the device moves into stronger inversion. This is reflected by lower variability for

R_{out2} compared to that of R_{out1} . DIBL variability has minimum impact on g_m variation. The variation in g_m is small and independent of gate bias.

3.2 New Modeling Approach

Fig. 3 shows model-silicon comparison for DIBL. The model variation is generated with the MC simulations using length, width and threshold voltage as random variables. It can be seen that the model doesn't produce any variations in DIBL especially at long channel lengths; whereas the data shows a significant amount of variation. This model deficiency results in underestimating R_{out} variations in the model compared to the data as shown in Fig. 4.

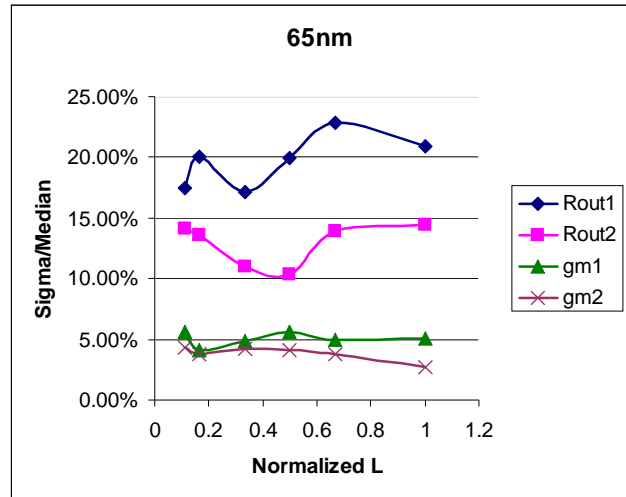
In order to provide more accurate R_{out} estimates, we propose a new and practical approach to incorporate large long channel DIBL in variation models. We provide a sub-circuit model with a VCVS in series with the gate. This voltage source imitates DIBL by providing additional gate-overdrive linearly proportional to the drain bias. Fig. 5 explains this concept through I_d-V_d curve. The VCVS impacts high V_{ds} region without affecting the linear region. The constant of proportionality for the voltage source is obtained from the data. With this new method, we are able to match DIBL and R_{out} variability in the data through our models as shown in Fig. 6 and 7. This method has an advantage over other methods as the same sub-circuit can be used on top of the core model.

4 CONCLUSIONS

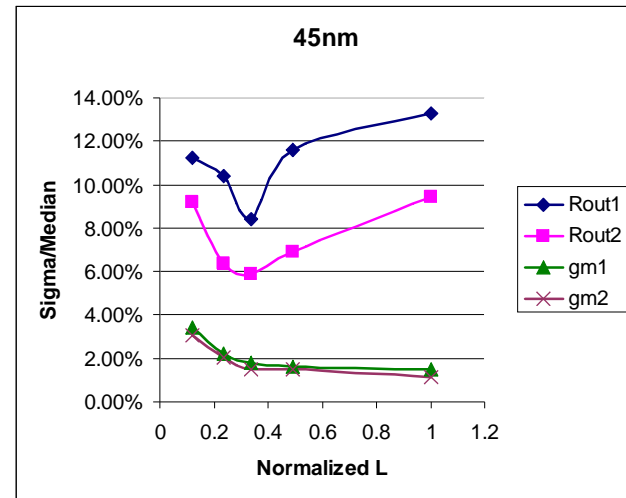
Out data analysis for 65nm and 45nm technologies showed that the variation in R_{out} at long channel depends very strongly on the variation in DIBL. We propose a new method to implement this DIBL variation in the corner models for accurate R_{out} estimation for analog design. The advantage of this method is that it is independent of the underlying BSIM parameters for a particular device. It is also very straightforward to adjust the spread in DIBL if any of the process/integration elements change it.

5 REFERENCES

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(a)



(b)

Fig. 1: Variability of g_m and R_{out} in 45nm and 65nm technologies.

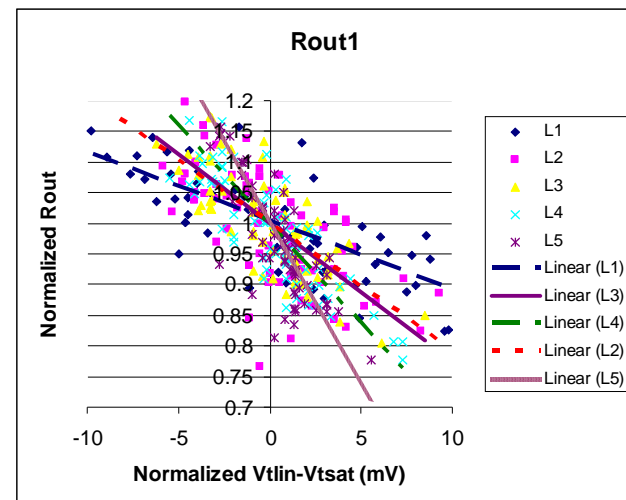


Fig. 2: Variation in R_{out} data plotted as a function of DIBL variation.

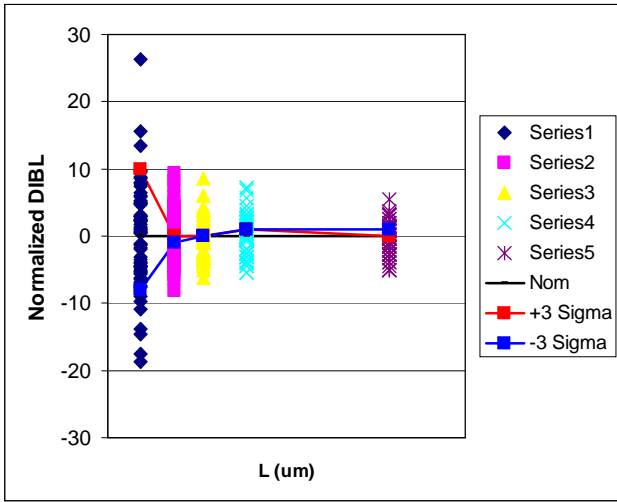


Fig. 3: Model-Si correlation of DIBL with existing variation modeling methodology.

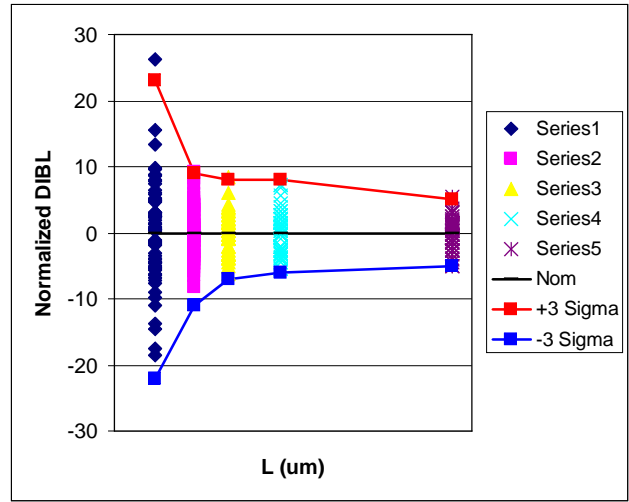


Fig. 6: Model-Si correlation of DIBL with new variation modeling methodology.

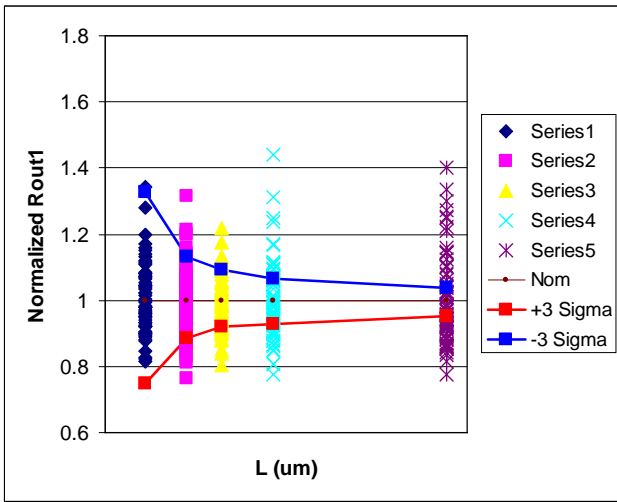


Fig. 4: Model-Si correlation of R_{out1} with existing variation modeling methodology.

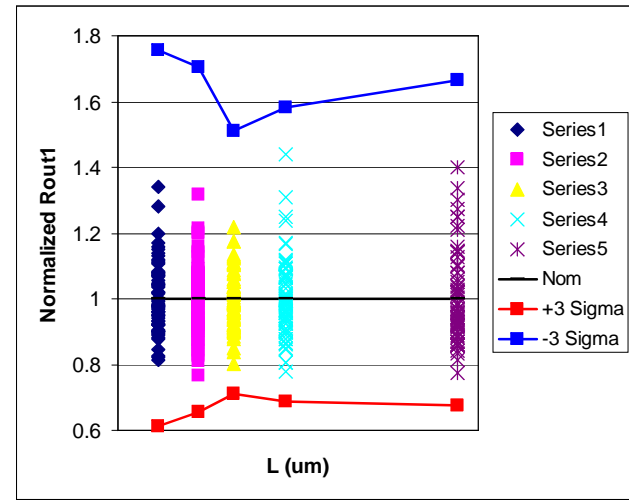


Fig. 7: Model-Si correlation of R_{out1} with new variation modeling methodology.

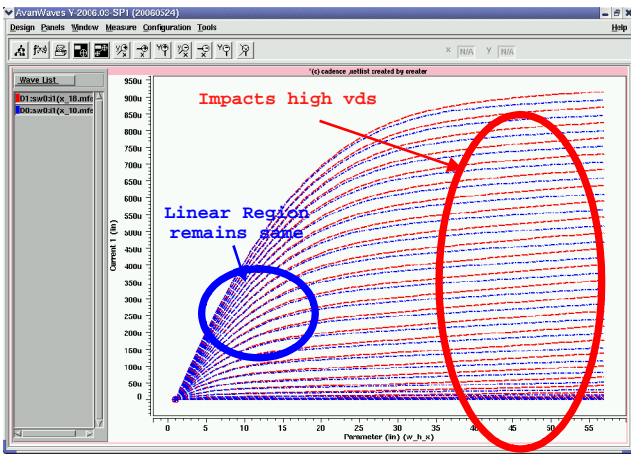


Fig.5: VCVS for the implementation of new variation modeling methodology. It imitates DIBL by providing additional gate voltage for high V_{ds} region.