Si-Based Process Aware SPICE Models for Statistical Circuit Analysis

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ABSTRACT

Process independent design methodologies are no longer going to be productive with the scaling of the device technology nodes into nanometer regime. Design and process are more tightly integrated for the better manufacturability. Critical link between the process and design is the compact model of the devices being used in a particular technology design, which will in-turn serves as a virtual fabrication house for the designer. This is possible, only if the compact model has process dependency information. In this paper, we will describe the methodology to create the process-aware compact models and validate the model using the 130 nm technology Silicon data at a) device level and b) circuit level. We have achieved good results in matching the silicon-measured data of a 3481 stage Ring-oscillator circuit with that of the extracted process-aware compact model for various process conditions.

Keywords: MOSFET Modeling, Process-Aware Compact Models, Circuit Simulation, TCAD.

1 INTRODUCTION

As CMOS technology is scaled, design dependent yield loss becomes increasingly important due to increasing interactions between design and manufacturing. The manufacturing variability can be too large to achieve performance goals by designing a chip only to SPICE corner models. This leads to a requirement of SPICE models that include process variations during manufacturing. Currently, process variations are imposed on models via statistical distribution of SPICE parameters. This approach suffers from several fundamental flaws: (a) the actual SPICE model parameters may deviate far from their underlying physics, as they often end up as fitting parameters to silicon data, (b) it is erroneous to treat SPICE parameters as statistically independent of each other and (c) SPICE parameters cannot be directly linked to any one specific process variation. The situation is worse, if principle component analysis (PCA) is used, as it represents a further abstraction of process variability and it may not be possible to give feedback to the process engineers on how a particular process variable is affecting some of the critical electrical parameters of the device.

A methodology of extracting a process aware model using TCAD simulations was presented in [2] and [3]. Pertinent compact model parameters were obtained as a polynomial function of process parameters. However, TCAD models are approximate and do not completely capture the underlying real process variations.

In this paper, we present a methodology that allows for process splits and actual silicon data to be used to extract SPICE model parameters as a polynomial function of process parameter variations i.e. silicon based "process aware" SPICE models were extracted. Validation of the constructed process-aware compact model is done at the device level and as well as at the circuit level by using a 3481 stage Ring Oscillator silicon results.

2 METHODOLOGY

In order to construct a process-aware compact model for circuit simulations, the first thing we need to have is a global compact model which will match all the I-V and C-V silicon data at all the bias conditions and device geometries of interest at nominal process conditions. Once we have a global compact model with acceptable accuracy, one can convert the global compact model into a process-aware compact model by following the below steps:

1. Select key model parameters which are directly related to the high sensitive process parameters for a given technology.
2. Add an extra term $f_{mpar}(P_1,P_2,P_3,\ldots,P_N)$ to the nominal value of the model parameter *mpar*; for example, in BSIM3 compact model, threshold voltage parameter VTH0 can be written as:

$$Vth0 = Vth0\_nominal + \Sigma\Sigma a_i^{(n)} P_i^n \qquad (1)$$

Where a_i (i=1,2,3…) are the coefficients whose values to be extracted by fitting the given I-V data for different process conditions, and the value of "n" can be selected depending on the variation of the electrical quantities with respect to the process conditions. For example, n=1 gives the linear dependence of process parameters on vth0 as given in Eq. 1, and n=2 gives the quadratic dependency.

3. Once we have extracted the process dependent key model parameters, validate the model with the silicon data for arbitrary values of the process parameters within the valid range of process parameters.
4. Next step is to check the predictability of the extracted compact model. This test should be done at device level and as well as at the circuit level.
   a) At device level, compare the Silicon I-V data with I-V obtained from circuit simulations using the extracted process-aware library file at process conditions different from the process conditions used for extraction of the model.
   b) Ring oscillator circuit delay is a perfect metric to be used for validating any compact model. Compare the delay obtained from the measurements on a fabricated ring oscillator with that of the simulated ones.
5. Once above tests are successfully completed then only the compact model can be used for designing circuits while considering the process variations. This way, one can design the circuits robustly with respect to process variations.

3 RESULTS

In this work, we have used Silicon I-V data of 130 nm technology node, and the compact model selected is BSIM3v3. For the global parameter extraction, we have used the devices with dimensions listed in Table 1 for both NMOS and PMOS devices.

W/L (um)	10	0.8	0.35	0.13
10.0	X	X	X	X
0.6	X	X	X	X
0.15	X	X	X	X

Table 1: Lists the value of Width and Length of the transistors being used for extracting the global model. "X" defines that we have included that device I-V data in the extraction process.

The extraction accuracy of the global model parameter extraction has been checked using RMS error on all the curves of all the devices being used. We have achieved total RMS error value less than 4 %. After extracting the model parameters by fitting all the given I-V data at various bias conditions for the given device dimensions, next step is to construct the process-aware compact model. For this purpose, we have used the I-V Silicon data for the process conditions mentioned in Table 2. Here, we have selected PolyCD and TOX as the process parameters for both NMOS and PMOS devices. Selection of the process parameters are done based on the sensitivity analysis of the process variables on the critical electrical parameters. In this particular case, we have found the variation of PolyCD and TOX values have maximum impact on the device characteristics compared to the variations on the other process parameters.

Device	NMOS		PMOS	
S. No.	PolyCD (nm)	TOX (A)	PolyCD (nm)	TOX (A)
P1	125	23.5	125	22
P2	108	23.5	125	24.5
P3	125	26	125	30
P4	125	29	125	27.5
P5	125	31.5	108	22
P6	142	23.5	142	22

Table 2 lists the process conditions used for the splits for a 0.13µm CMOS process.

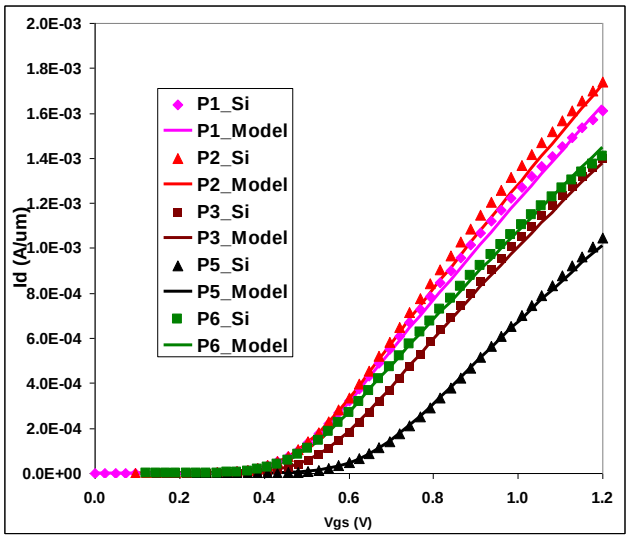

Fig. 1: IdVg (Vds=0.1 V) Model vs. Measured for process conditions shown in Table 1; NMOS 10x0.13.device.

We have chosen the quadratic dependence of process parameters on the model parameters (i.e., n=2 in Eq. 1). We have extracted the coefficients for the chosen key model parameters by fitting the I-V data for the process conditions given in Table 2.

The quality of the extraction process is shown in Figs. 1 and 2. Fig.1 shows the IdVg curves in linear region of operation for the process conditions given in Table 2 for NMOS device of W/L 10x0.13 um. Similarly, Fig.2 shows the IdVg curves in linear region of PMOS device. As seen from the figures, the extraction quality has been reasonable good, the error between the simulated and Silicon data is less than 3 %.

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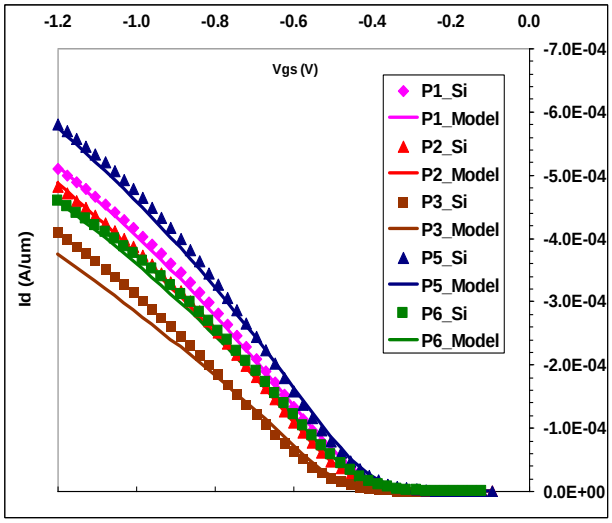

Fig. 2: IdVg (Vds=-0.1 V) Model vs. Measured for process conditions shown in Table 1; PMOS 10x0.13.

The robustness of this methodology was tested by the quality of fits to the silicon devices and data for process conditions not used in the extraction as shown in Figures 3-6 for both PMOS and NMOS devices. Figs. 3 and 4 shows the IdVg and IdVd characteristics, respectively, of NMOS device with PolyCD values 117 nm and 134 nm. Note that the devices with these PolyCD values were not used in the extraction process. However, we see a good match between the Silicon data and the simulated I-V curves. This shows the predictability of the process-aware model at the device level. Similarly, Figs. 5 and 6 show the I-V curves of PMOS device at two different PolyCD values. Good accuracy in matching with the Silicon I-V data can be observed here.

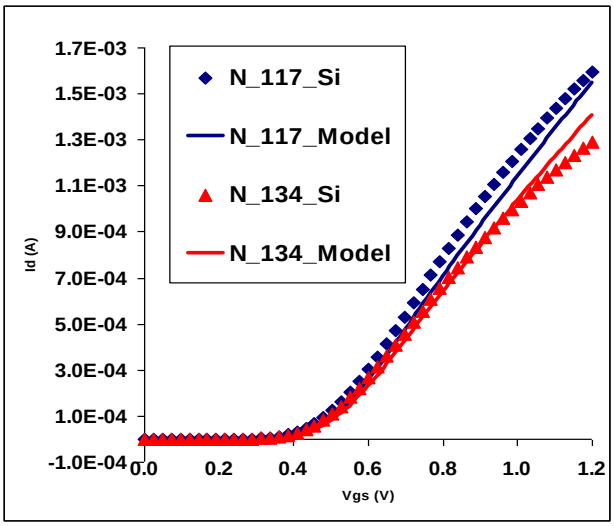

Fig. 3: IdVg (Vds=0.1 V) Model vs. Measured; NMOS for different PolyCD values.

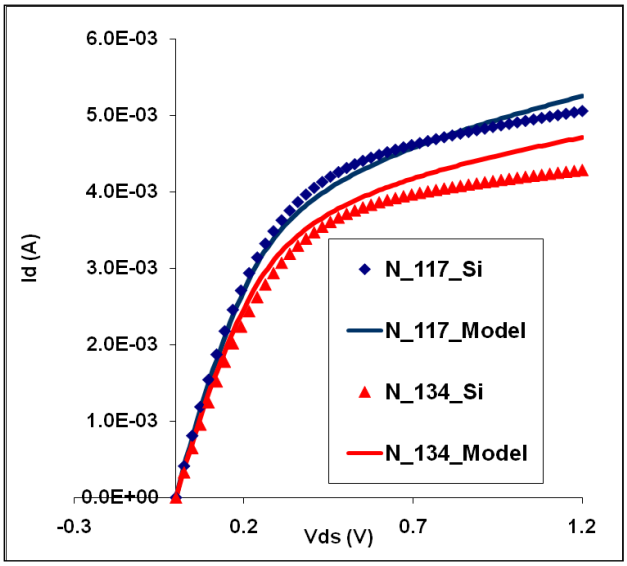

Fig. 4: IdVd (Vgs=1.2 V) Model vs. Measured; NMOS for different PolyCD values.

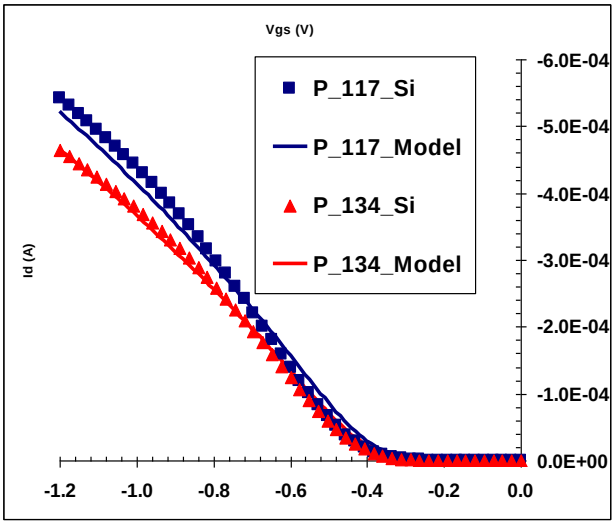

Fig. 5: IdVg (Vds=-0.1 V) Model vs. Measured; PMOS for different PolyCDvalues.

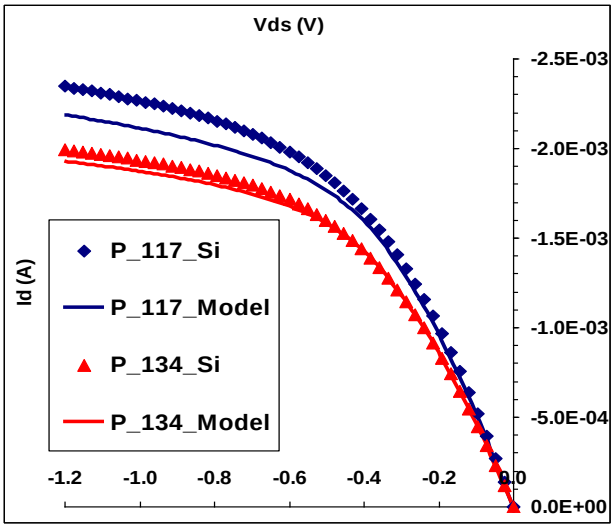

Fig. 6: IdVd (Vgs=-1.2 V) Model vs. Measured; PMOS for different PolyCD values.

A further test of quality of this approach was based on the predictive capability of the model on the performance of a simple circuit. Figure 7 shows the excellent fit between the measured period and the prediction from the process aware SPICE model for a 3481-stage Ring Oscillator circuit.

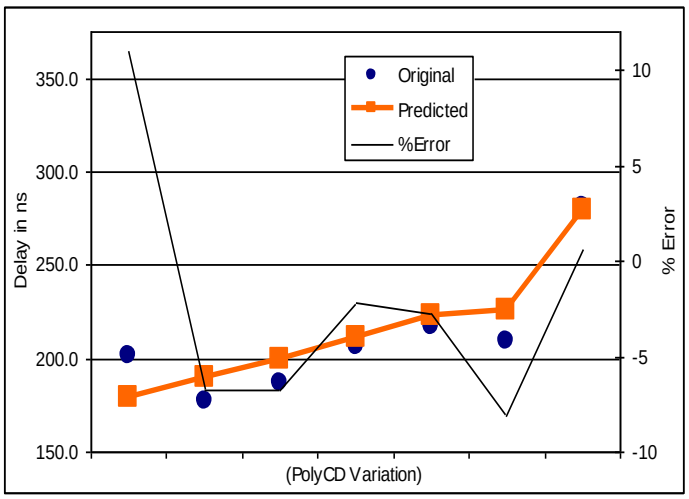

Fig. 7: 3481 Stage Ring Oscillator Circuit time period as obtained from measurements and HSPICE simulations using the process-aware compact model for different PolyCD; Right Y-axis shows the % error between the simulations and measurements.

4 SUMMARY

In this paper, we have demonstrated the methodology to construct the process-aware compact models. Also, we have presented the validation of the extracted model using the Silicon data at device and circuit. Process-aware SPICE models enable engineers to optimize process and design and minimize split lot experiments to identify maximum performance point for a given design. It also provides more control over the existing area, power and performance related constraints, to help optimize for a robust design.

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