Process Aware Compact Model Parameter Extraction for 45 nm Process Flow

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ABSTRACT

CMOS devices are simulated using a 45-nm process flow that uses advanced techniques to achieve the requisite performance. The process parameters with maximum impact on the device characteristics are identified and analyzed. Global and process-aware model parameters are extracted for the 45-nm process. A five-stage ring oscillator is examined to demonstrate the effects of process variability on circuit performance. Good agreement between the model and the numeric simulations is observed demonstrating the robustness of the extraction methodology and the process-aware model parameters.

Keywords: parameter extraction, process-aware compact models, design for manufacturability

1 INTRODUCTION

In the semiconductors industry, the device geometries decrease and the integration densities increase with each technology node. Designing and manufacturing circuits with smaller device geometries is a major challenge for the microelectronics industry because of the process variability impact on device and circuit performance, leading to lower reliability and yield [1], [2].

To design robust circuits using deep sub-micron devices, the effects of process variability on the circuit model parameters must be examined in detail. A thorough assessment of the process variability impact on the circuit model parameters leads to better designs, improved manufacturability and higher yield. In this paper, methodologies to extract circuit model parameters that account for process variability are demonstrated. Strategies to account for the process variability induced circuit performance variation are also developed.

2 NUMERIC SIMULATIONS

The process simulations for the CMOS devices are performed using a 45-nm process flow that uses high-k gate dielectric with an effective oxide thickness (EOT) of 0.812 nm, halo and source/drain implants, stress engineering and spike and laser anneals to attain the requisite performance. Table 1 shows key parameters for the devices simulated using the 45-nm process flow.

	NMOS	**PMOS**
L_{gate} [nm]	45	45
I_{on} [mA/μm]	1.207	-0.3482
I_{off} [μA/μm])	1.407×10^{-3}	-8.595×10^{-4}
G_m [mS/μm]	0.5610	0.1292
V_{th} [V]	0.3453	-0.4381
V_{dd} [V]	1.0	-1.0

Table 1: 45 nm technology parameters

The process parameters for the NMOS and PMOS devices are adjusted to match the electrical performance. Electrical characteristics are simulated using simple drift diffusion models [3]. It can be observed from the device characteristics presented in Table 1 that these devices are appropriate for low power applications, since the PMOS characteristics exhibit a low on current (I_{on}) accompanied by a significantly lower off current (I_{off}).

The compact model parameters are extracted using the BSIM4 MOSFET model [4]. Two sets of process simulations are performed to estimate the global and process-aware model parameters. Global parameters are extracted for the 45-nm process with drawn gate lengths from 32 nm to 1 μm. The process-aware model parameters are extracted from simulations where process parameters like gate length, gate taper angle, halo dose and halo energy are varied. These parameters are selected to model the process variability because of their greater impact on the electrical characteristics. The gate oxide thickness is not varied as the gate oxide is a combination of SiO_2 and HfO_2. Parameter extraction is performed using a specialized parameter extraction tool that can directly generate process-aware compact models [5].

3 PARAMETER EXTRACTION

Process and device simulations are performed using a 45-nm process flow to extract the global model parameters. For these simulations, the drawn gate length is varied from 32 nm to 1 μm and the other process parameters are kept constant. Figure 1 shows the variation of the threshold voltage (V_{th}), calculated in the linear region, and the transconductance (G_m) with respect to gate length; and Figure 2 shows the variation of the on and off currents (I_{on} and I_{off}) with gate length for PMOS and NMOS devices.

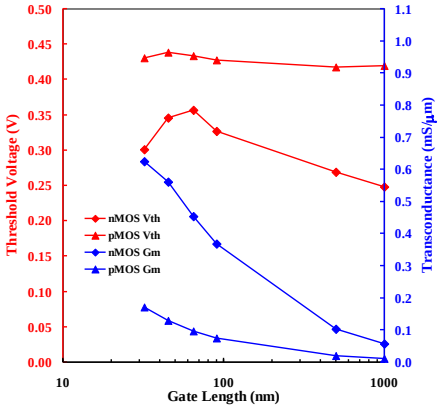

Figure 1: V_{th} and G_m with respect to L_{gate}.

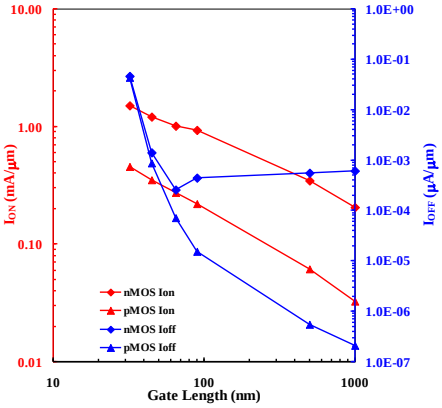

Figure 2: I_{on} and I_{off} as functions of L_{gate}.

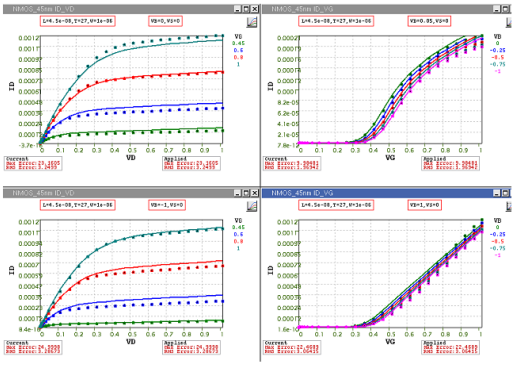

Figure 3: I-V characteristics for NMOS with L_{gate} = 45 nm.

The global model parameters represent the nominal process conditions and various drawn gate lengths. Figure 3 shows the current-voltage characteristics for a 45-nm NMOS device. The points show the numeric simulation data and the solid lines show the electrical characteristics generated by the global SPICE model. Similarly, Figure 4 shows the comparison between the simulation results and the global model for a 45-nm PMOS device. The global SPICE model extracted here shows an RMS error of ~4%.

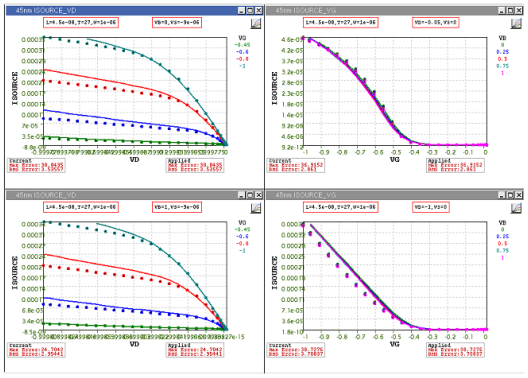

Figure 4: I–V characteristics for PMOS with L_{gate} = 45 nm.

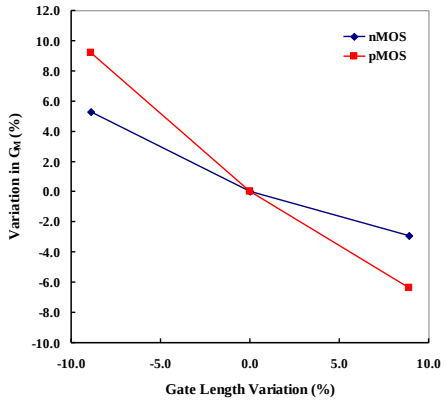

Figure 5: G_m variation with respect to L_{gate} variation.

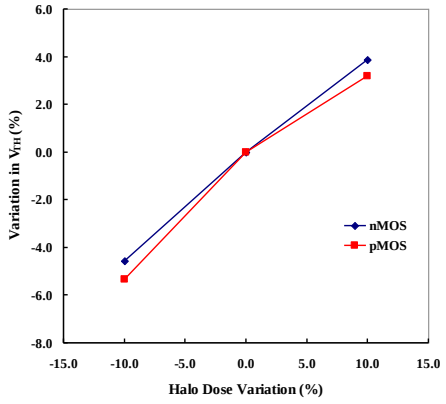

Figure 6: V_{th} variation with respect to halo dose variation.

To extract the process-aware model parameters, gate length, gate taper angle, halo dose and halo energy are varied around their nominal values. Figure 5 shows the variation in the NMOS and PMOS transconductance with respect to the gate length variation. Similarly, Figure 6 shows the threshold voltage variation with respect to the halo dose variation. These figures clearly show the impact of process variability on the device characteristics. The process-aware model is based on the global model and the process variability induced performance variation.

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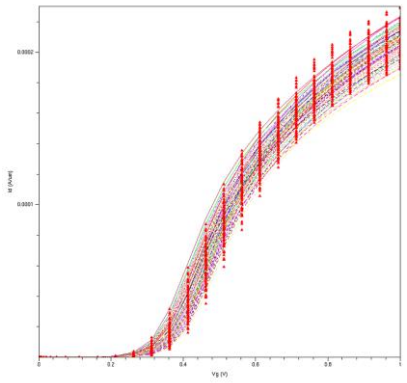

Figure 7: NMOS I_d–V_g at V_d = 0.05 V and V_b = 0.0 V.

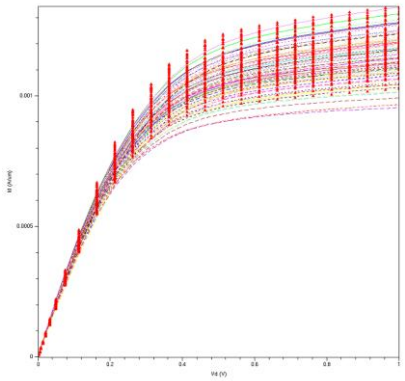

Figure 8: NMOS I_d–V_d at V_g = 1.0 V and V_b = 0.0 V.

Figure 7 shows the I_d-V_g characteristics of the NMOS devices with a drain voltage of 0.05 V and a bulk voltage of 0.0 V. The lines show the electrical characteristics obtained from the TCAD simulations and the dots show the behavior predicted by the process-aware model. Similarly, Figure 8 shows the I_d-V_d characteristics at a gate voltage of 1.0 V and bulk voltage of 0.0 V. These figures clearly indicate that the process-aware model developed here can account for process variability induced performance variation.

4 CIRCUIT MODELING

Simple digital circuits, like the five-stage ring oscillator shown in Figure 9, are simulated to assess the accuracy of the extracted circuit model parameters. Mixed mode TCAD simulations are compared with circuit simulations performed using the process-aware model parameters [6]. In addition, the absolute model error is calculated using:

$$Error = \frac{Q_{SPICE} - Q_{TCAD}}{\sqrt{\sum (Q_{TCAD})^2 / N}} \quad , \qquad (1)$$

which indicates the model accuracy. These studies demonstrate the accuracy and the robustness of the process-aware circuit model parameters.

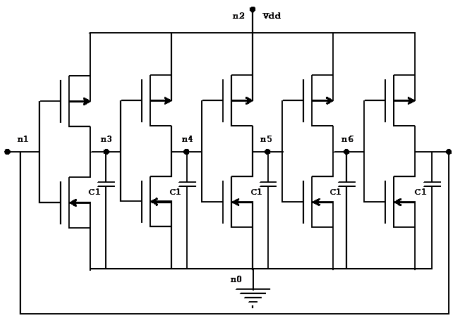

Figure 9: Five-stage ring oscillator.

For the five-stage ring oscillator studied here, mixed mode TCAD simulations are compared with HSPICE® simulations performed using the process-aware model parameters. For the HSPICE® simulations, a load capacitor of 5.0×10^{-15} F is added at each inverter output to account for the device capacitances. Figure 10 shows the variation of the ring oscillator power dissipation with respect to the gate length. The error bars represent an error of 15% in the model.

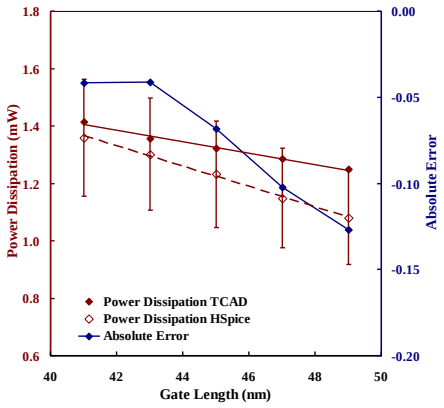

Figure 10: Power dissipation as a function of gate length.

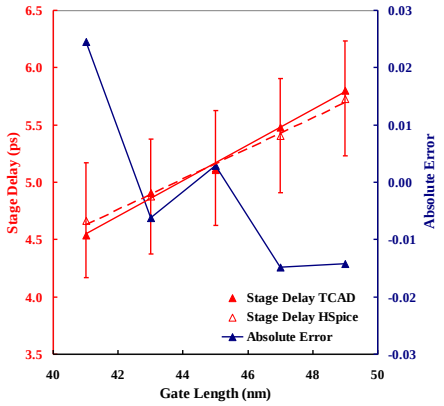

Figure 11: Stage delay as a function of gate length.

Figure 11 shows the variation of the stage delay with respect to the gate length. Figure 12 shows the variation of

ring oscillator frequency with respect to the gate length. In case of Figures 11 – 12, the error bars represent an error of 5% in the model.

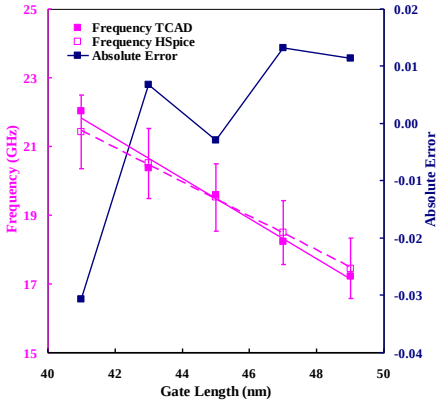

Figure 12: Frequency as a function of gate length.

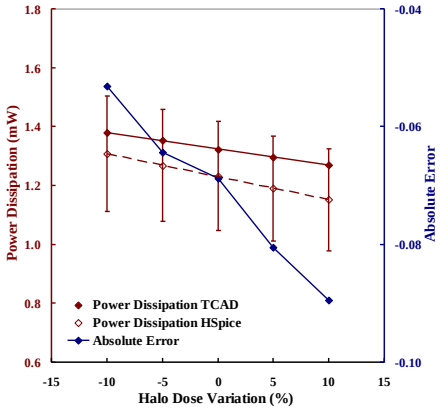

Figure 13: Power dissipation versus halo-dose variation.

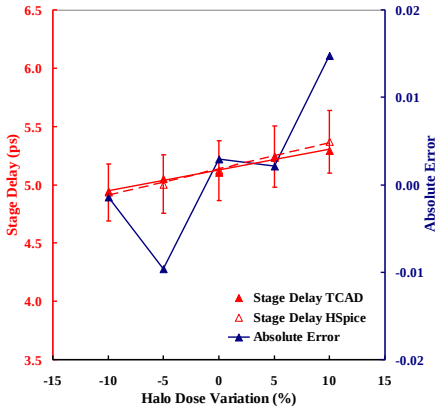

Figure 14: Stage delay as a function of halo dose variation.

Simulations are also carried out for variations in halo dose. Figure 13 shows the variation of ring oscillator power dissipation as a function of halo dose variation. The error bars show an error of 15% in the model. Figure 14 and Figure 15 show the variation of stage delay and frequency as functions of halo dose variation, respectively. Here, the error bars show an error of 5% in the model.

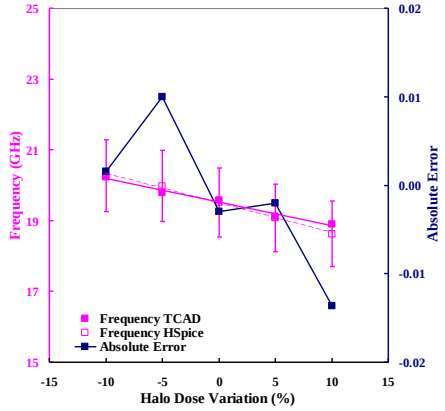

Figure 15: Frequency with respect to halo dose variation.

For Figure 10 – 15, the solid markers represent the mixed mode TCAD results and the hollow markers show the HSPICE® results. The absolute error is also plotted for the five-stage ring oscillator studied here. The results discussed so far show that the process-aware model can accurately predict the behavior of standard cells as well as more complex circuit elements.

5 CONCLUSIONS

Manufacturing process variability is a major cause of parametric yield loss. The process variability needs to be taken into account in order to improve the overall yield. Here, a methodology to extract process-aware model parameters and to create robust circuit designs that account for process variability is presented. The ring oscillator results discussed here show that the process-aware models can accurately predict the process variability impact on the performance of complex circuit elements.

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