# Nano-Gap High Quality Factor Thin Film SOI MEM Resonators

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## ABSTRACT

Silicon micro-electro-mechanical (MEM) resonators on a 1.25 µm thin SOI substrate are demonstrated to achieve quality factors of 100 000 at 24.6 MHz. Based on a improved fabrication process, 200 nm wide transduction gaps are fabricated, resulting in a strong electrostatic coupling at low bias voltages. Consequently, the motional resistance of the thin resonator is as low as 55 kΩ with a bias voltage of 18 V and values still below 100 kΩ are measured at 14 V.

***Keywords***: micromachining, resonator, quality factor, microelectromechanical system, electrostatic devices

## 1 INTRODUCTION

Miniaturization of silicon micro-electro-mechanical (MEM) resonators and co-integration with silicon ICs are main driving forces for the extensive research in this field. Performance characteristics of such miniaturized devices on par with quartz resonators have been demonstrated, mainly on thick substrates [1-3] to reduce the impedance levels and to achieve high quality factors, which in some cases exceed 100 000 [1,3]. Further impedance reduction is obtained with sub-micrometer gaps, using either sacrificial layer etching [2,4] or deep reactive ion etching [5-7] to reach dimensions below what can by obtained by lithographic structuring. Even though such remarkable results have been obtained, most demonstrated integrations for oscillator circuits rely on a two-chip solution [8]. In this work, we build resonators on thin SOI substrates, which will eventually lead to a single chip solution [9]. Such a co-integration will substantially increase the impact of MEM resonators on the RF circuit design. This paper presents the fabrication and the characterization of such 1.25 µm thin resonators with quality factors above 100 000 at 24.6 MHz.

## 2 DESIGN

The resonator body is made of longitudinally vibrating beams [1] connected in parallel, hence the name parallel beam resonator (PBR). The single beams are 161 µm long, 5 µm wide and separated by 5 µm. The beams are mechanically coupled to avoid independent movements, resulting in one single frequency. The mode shape of the resonator was verified with ANSYS and a synchronous movement of all beams is obtained for the design (Fig. 1). The two resonator designs studied vary by the number of beams connected in parallel and thus their total width. One resonator is 115 µm (12 beams) wide, called PBR 115, and the other has a total width of 195 µm (20 beams), called PBR 195. The parallel beams move in a free-free mode with one nodal point at the center, at which location the anchors are placed on the outermost beams.

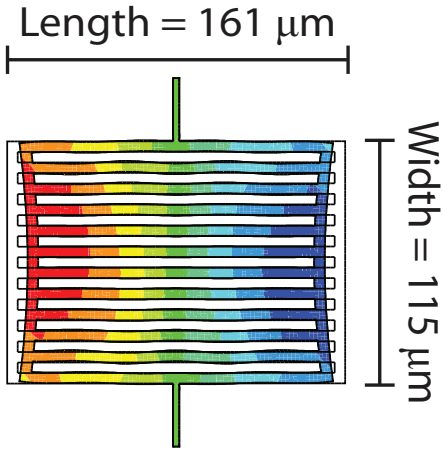


Figure 1: Mode shape of a PBR 115 resonator at its minimum position, simulated with ANSYS. The black line indicates the undeformed shape.

## 3 FABRICATION

A novel fabrication process of the resonators is described in Fig. 2. The SOI substrate has a 3 µm thin buried oxide and a 1.5 µm thin silicon film with a (100) surface orientation. A hardmask is created on top of the SOI wafer to define the nano-gap according to the method reported [6,7], where the gap is defined by a deposited thin polysilicon layer (Fig. 2a). This process reduces the total thickness of the SOI silicon film from 1.5 µm down to 1.25 µm. The transfer of the hardmask into the SOI device layer is done with a high aspect-ratio SHARP process (Fig. 2b). After releasing in BHF, the structures are dried in a $CO_2$ supercritical point dryer to avoid sticking and a thermal oxide is grown on the silicon surface (Fig. 2c). A CVD deposited parylene-C layer protects the suspended structures during the following steps, in which openings are etched with an isotropic ICP etch process (Fig. 2d). The top $SiO_2$ layer and the polysilicon layers are etched on the

electrodes and titanium is evaporated onto a two-layer lift-off resist to structure the metal contacts (Fig. 2e). Finally, the resonators are released in an isotropic oxygen plasma (Fig. 2f), which completely removes the parylene layer.

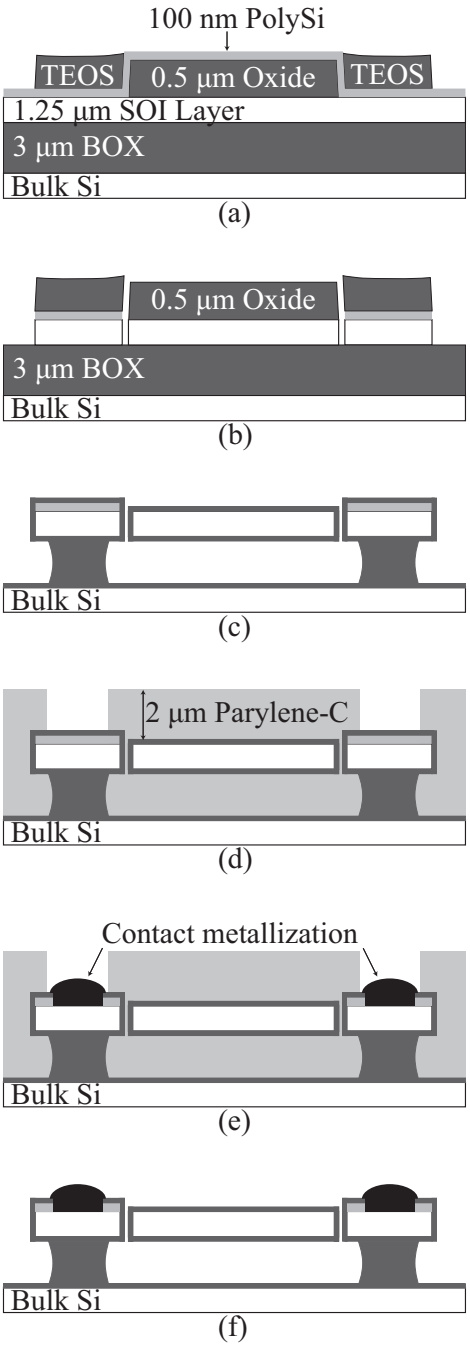


Figure 2: Process flow: (a) A hard mask is prepared, based on a sacrificial layer process (TEOS: Tetra-ethyl-ortho-silicate) (b) followed by a DRIE process. (c) Once released in BHF, $CO_2$ supercritical point drying avoids sticking and a dry thermal oxide is grown. (d) CVD deposited parylene protects the resonator during contact opening and (e) metallization followed by (f) an $O_2$-plasma release.

The released resonators are inspected after fabrication with an optical profilometer. These measurements indicate a stress-free completely flat surface for thin oxides grown on the silicon (Fig. 3).

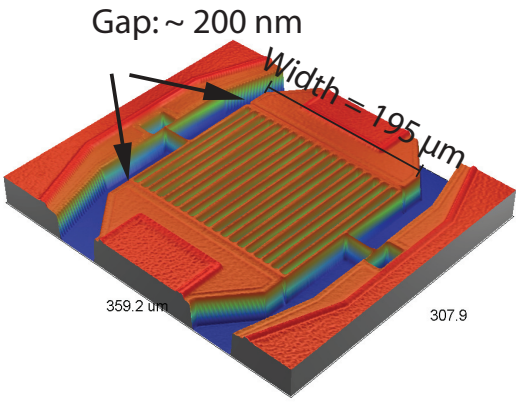


Figure 3: Fabricated parallel beam resonator image taken with an optical profilometer.

## 4 EXPERIMENTAL RESULTS

The resonators are characterized with a vector network analyzer and a decoupled DC source (Fig. 4). All measurements are taken in a SUSS cryogenic prober chamber, PMC150, under vacuum conditions better then $10^{-5}$ mbar. This equipment also enables us to test the temperature dependence of the different parameters of interest.

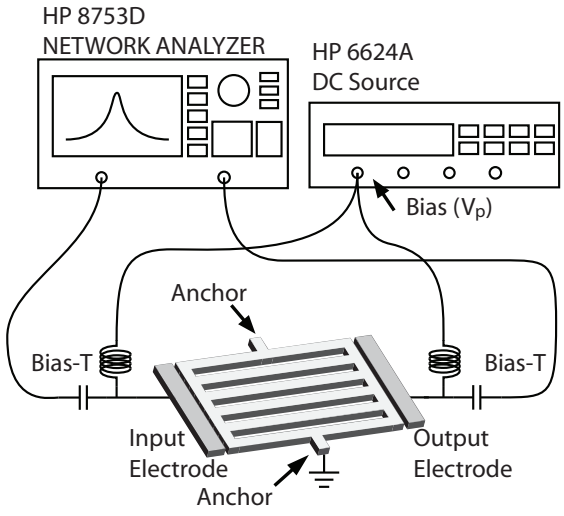


Figure 4: Measurement setup used for the two-port characterization of the parallel beam resonators.


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To avoid vertical pull-in of the resonator onto the substrate, both the bulk silicon and the resonator are grounded. The bias voltage ($V_p$) is applied through a bias-T on the electrodes to protect the virtual network analyzer.

Fig. 5 shows the scattering parameter S12 for a PBR 195 resonator at a bias of 20 V. The input RF power is -40 dBm. The quality factor is 100 000 with a motional resistance of 55 kΩ at a bias voltage of 18 V. Higher voltages result in a pull-in of the resonator onto the electrode and destruction of the device, reason for the limited tuning range of the motional resistance with the bias voltage. A series of four measurements taken on a second structure of the same type results in a motional resistance of 64 kΩ (Fig. 6) with $V_p$=14 V, pointing to the high sensitivity of this parameter on gap fabrication tolerances.

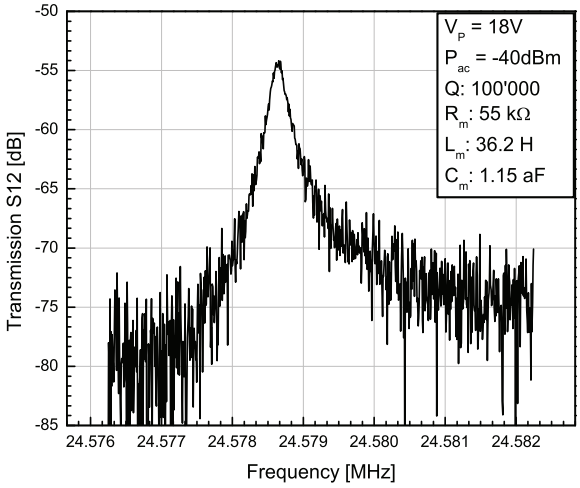


Figure 5: S-parameter measurement of a PBR 195. A quality factor of 100’000 and a motional resistance of 55 kΩ is measured with $V_p$=14 V.

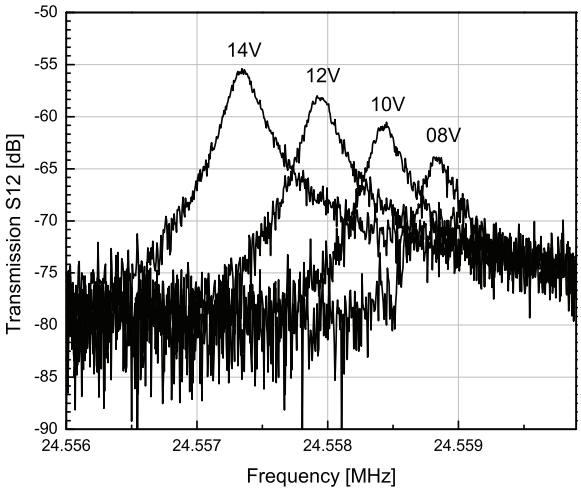


Figure 6: S-parameter of a PBR 195 as a function of bias voltage: the motional resistance is 64 kΩ , with $V_p$=14 V.

The smaller design PBR 115, with 12 beams, has a very similar transfer characteristic. The measurement in Fig. 7 is taken with a RF power of -30 dBm at bias voltage from 12 V to 20 V. The quality factor is 70 000, lower then for the PBR 195 and the motional resistance is 120 kΩ with $V_p$=20 V. This higher equivalent impedance level is explained by the smaller electrode surface and the lower Q-factor of the resonator, compared to the PBR 195.

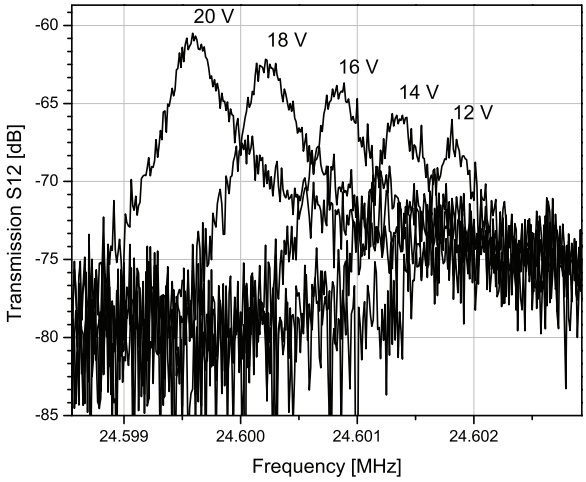


Figure 7: Measured frequency spectra of a PBR 115 with varying bias voltage; $R_m$=120 kΩ with $V_p$=20V.

Based on the frequency versus bias voltage characteristics (Fig. 8), an effective gap is extracted through fitting of a resonator model to the measured data. The gap size was found in the range of 190 nm to 210 nm, which corresponds well to the observed motional resistance values. The frequency tuning of the resonator with bias voltage, as given in Fig. 8, is depending on the gap size. For the measured structures the total frequency tuning is >2.5 kHz over a range of 10 V. The difference of the motional resistance for two PBR 195 structures is explained by a difference in effective gap size of 7 nm, due to process variations during the gap etching.

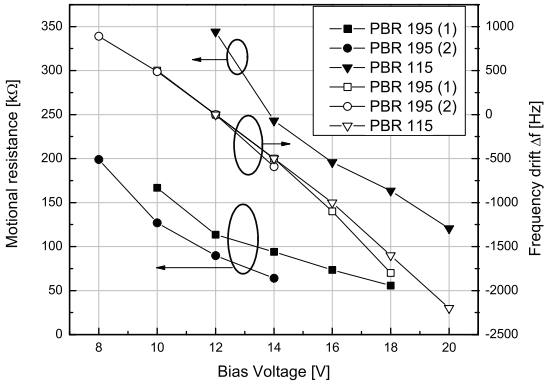


Figure 8: The motional resistance and the frequency tuning versus the bias voltage for three structures. Process variations are strongly influencing the motional resistance of the resonators (PBR 195).

Frequency stability with temperature is an important parameter for any resonator in industrial applications. Fig. 9 gives a comparison of the resonator behavior with respect to temperature for one resonator of each type from 160 K up to 380 K at an interval of 20 K. Both measured resonators behave vary similar, showing a frequency drift which averages at 15.7 ppm/K and 15.3 ppm/K for PBR 115 and PBR 195 respectively, lower then expected from previous results [7].

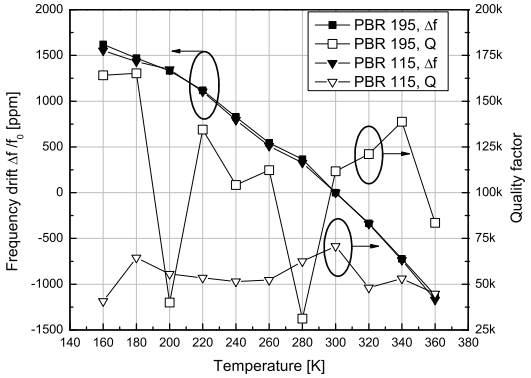


Figure 9: Variation of the resonance frequency and the quality factor with temperature. An unidentified problem caused low Q-factors at 200 K and 280 K for the PBR 195.

The quality factor was extracted for the measurements performing a fit of a Lorentz function to approximately 100 data points around the resonance peak. Even though this method was shown to reduce the influence of noise on the result [10], an unidentified problem occurred on two data points with Q-factors below 40 000 for the PBR 195. Overall, an increasing Q-factor with decreasing temperature is observed, but the precision of the measurement is limited. For the PBR 115 a rather linear trend over the whole temperature range is found, with values for the most part above 50 000.

## 5 CONCLUSION

A CMOS compatible fabrication process for 1.25 µm thin SOI MEM resonators is presented showing the feasibility to construct resonators with quality factors above 100 000 in thin SOI. The motional resistance is as low as 55 kΩ measured with a low bias voltage of 18 V. Characterization of the resonators in a broad temperature range shows a constantly high quality factor and frequency drift which is dominated by the silicon thermal properties. These results implicate that co-integration of electrostatic MEM resonator and CMOS circuits on thin SOI substrates can be done with extremely high quality factors.

## ACKNOWLEDGEMENT

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