HiSIM-LDMOS/HV: A Complete Surface-Potential-Based MOSFET Model for High Voltage Applications

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ABSTRACT

We present here the high-voltage MOSFET model HiSIM-LDMOS/HV based on the complete surface-potential description. The model is valid both for symmetrical and asymmetrical device structures, has accurate scaling properties for structural variations such as gate wide, gate length or drift-region length and is valid for a wide range of bias conditions. The predictability of the developed model is discussed with examples of various device parameter variations.

Keywords: surface potential, resistance, LDMOS, HVMOS, circuit simulation

1 INTRODUCTION

High-voltage MOSFETs are becoming important due to expanding utilization of integrated circuits for high-voltage requirements such as in many automotive of mobile applications. Necessary voltage-handling capabilities extend from a few volts to several hundred volts. This wide range of the operation conditions is realized with a low impurity concentration region, called drift region. To achieve the capabilities for high voltage applications, two structures have been developed. One is the laterally diffused asymmetric MOSFET (LDMOS) as shown in Fig. 1a [1]. The other is the symmetrical high-voltage MOSFET (HVMOS) as shown in Fig. 1b.

It has been observed that the capacitances of LDMOS devices show specific complicated features as a function of applied voltages. Namely, strong peaks are observed in C_{gg} as a function of the gate voltage V_{gs} (see Fig. 2). Previously, modeling has been done either by introducing an internal node at the channel/drift junction [2] or with a resistance in a macro model [3]. The former approach solves the node potential iteratively until the channel current and the current in the drift region at the internal node become equal. Recently, the LDMOS features have been modeled by considering the potential drop in the drift region in a consistent way by directly solving the device equations with an iterative approach [4]. Our investigation here mainly aims at extending the LDMOS model to including the symmetrical case, which is also important for high-voltage MOSFET optimization. The extended model is called HiSIM-LDMOS/HV.

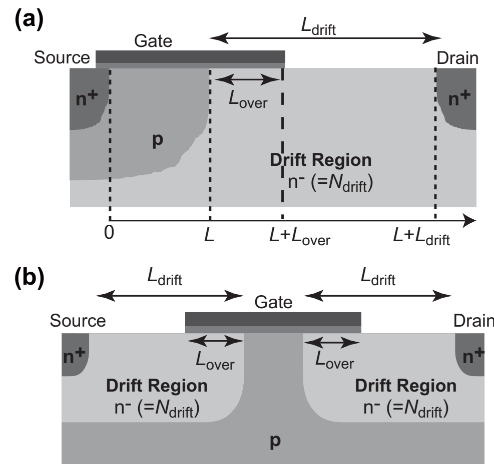

Fig. 1. Cross-sections of the studied LDMOS (a) and HVMOS (b) devices.

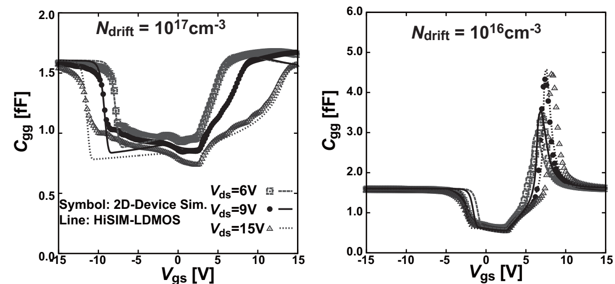

Fig. 2. Capacitance comparison between 2D-device simulator (symbols) and developed compact model (lines) results for the LDMOS structure with different drift-region doping of 10^{17}cm^{-3} (left) and 10^{16}cm^{-3} (right).

2 LDMOS CHARACTERISTICS

The channel part of the LDMOS device is formed by out-diffusion of the impurity concentration from the source contact region. The drift region is usually formed by the substrate. On the other hand, HVMOS has the conventional MOSFET structure, but with long drift regions at both source and drain. The resistive drift region for providing the high-voltage capability, namely its length L_{drift} and its doping concentration N_{drift}, determine important operational properties of the LDMOS/HVMOS device.

Figs. 3a-c show comparisons of *I*-*V* and g_m characteristics for two impurity concentrations in the drift region N_{drift}, while keeping the length L_{drift} and other model parameters the same [4]. Corresponding C_{gg} characteristics are compared for the two different N_{drift} values in Fig. 2. The anomalies observed for reduced N_{drift} in C_{gg} are caused by the increased resistance effect in the drift region due to the lower impurity concentration, which coincide with drastic reduction of g_m, as obvious from Fig. 3b.

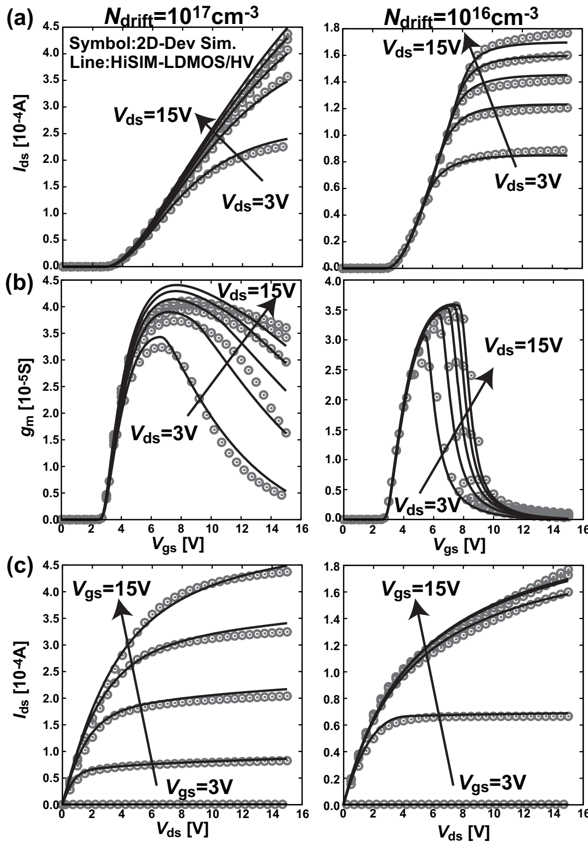

Fig. 3. *I*-*V* and g_m comparison between 2D-device simulator (symbols) and developed compact model (lines) results for the LDMOS structure with different drift-region doping of 10^{17}cm^{-3} (left) and 10^{16}cm^{-3} (right).

To model the resistance effect of the drift region in a consistent way, the iterative Poisson-equation solution for the surface potentials in the MOSFET channel is extended to include the resistance effect of the drift region. The respective potential drop is written as

$$\Delta V = I_{ds} * R_{drift} \qquad (1)$$

where the resistance in the drift region is denoted as R_{drift} [5]. This potential drop is treated as the reduction of the applied voltages. Fig. 4 shows a calculated potential distribution denoting also the potential drop in the drift region. The influence of the resistance on the potential node at the channel/drift junction is summarized in Fig. 5. The specific features of the LDMOS structure can be exactly seen in this comparison. With negligible resistance in the drain contact, the potential $\phi_{s(\Delta L)}$ at the junction between MOSFET channel and drift region increases nearly linearly up to $\phi_{s0} + V_{ds}$, where ϕ_{s0} is the potential at source and is about equal to unity under the strong inversion condition [6]. The resistive drift region causes a potential drop as I_{ds} increases with larger V_{gs}. Under this condition, the potential value $\phi_{s(\Delta L)}$ even decreases while V_{gs} is increasing as can be seen in Fig. 5a. The described effect for the potential causes the anomalous features of the LDMOS device behavior.

Fig. 5b compares calculated $\phi_{s(\Delta L)}$ with HiSIM-LDMOS/HV and with a 2D-device simulator as a function of V_{ds}. Under the saturation condition the potential is expected to saturate. However, $\phi_{s(\Delta L)}$ continues to increases gradually due to the resistance effect. This continuous increase of $\phi_{s(\Delta L)}$ under the saturation condition results in the quasi-saturation behavior of LDMOS devices, with gradually increasing drain current, even beyond the saturation condition for the MOSFET.

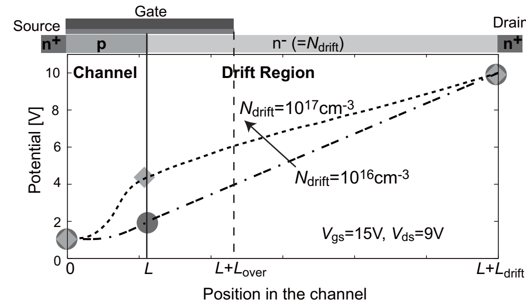

Fig. 4. Calculated potential distribution along the channel with the developed HiSIM- LDMOS/HV model (shown with symbols) for two N_{drift} concentrations. Lines are 2D-device simulation results.

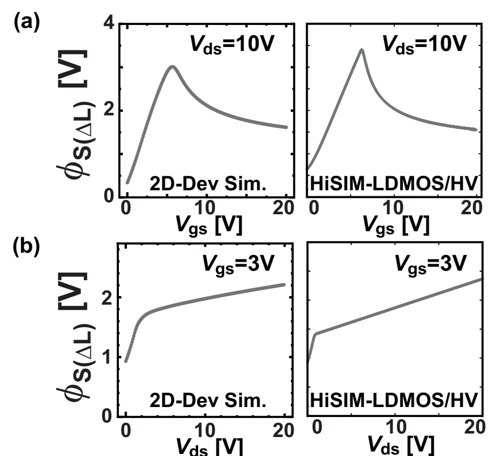

Fig. 5. Comparison of calculated surface potential at the channel / drift region junction with a 2D-device simulator and HiSIM-LDMOS/HV, (a) as a function of V_{gs}, and (b) as a function of V_{ds}.

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3 EXTENSION TO THE SYMMETRICAL HVMOS DIVECE

For symmetrical HVMOS modeling, the resistance model is applied to the source side as well. Fig. 6 shows a calculated potential drop within the source causing the reduction of V_{gs} to V_{gseff}. This additional potential drop results in the reduction of V_{ds} and V_{bs} as well. Therefore, the influence of the source resistance is expected to be drastic.

Accurate modeling of the overlap charge, Q_{over}, becomes more important for the symmetrical HVMOS device due to its increased contribution to the operational characteristics. For this accuracy purpose the bias dependent surface potentials within the overlap region have to be considered in describing the formation of the accumulation, the depletion or the inversion condition underneath the gate overlap region, which now depend in a complicated way dynamically on bias conditions. There modeling tasks are achieved by solving the Poisson equation in the same way as in the channel. The overlap charges are determined with the calculated surface potential distribution under the approximation that the potential variation along the overlap region is negligible. The surface-potential values are of course a function of N_{drift}, which determines also the flat-band voltage within the overlap region. Calculated overlap capacitances are shown in Fig. 7 as a function of V_{gs}.

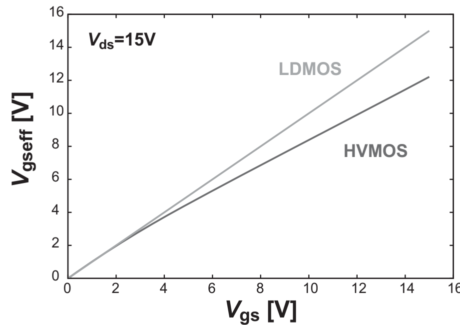


Fig. 6. Comparison of the effective gate-source voltage (V_{gseff}) as a function of the applied gate-source voltage (V_{gs}) for the symmetrical HVMOS and the LDMOS device structures.

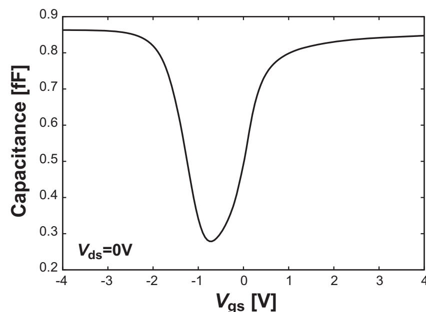
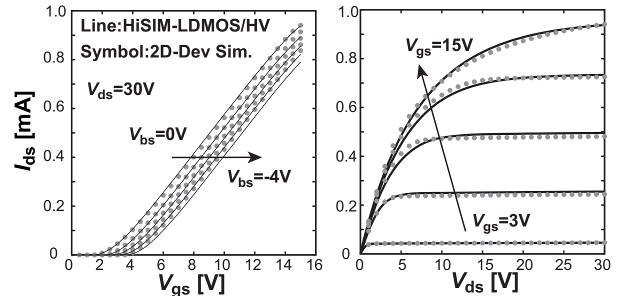


Fig. 7. Calculated overlap capacitance at the drain side with HiSIM-LDMOS/HV at V_{ds}=0V.

4 RESULTS AND DISCUSSIONS

Figs. 8a,b compare calculated *I-V* characteristics of HiSIM-LDMOS/HV for LDMOS and symmetrical HVMOS with 2D-device simulation results, respectively. The high resistance effect of the drift region causes a reduction of the potential increase in the channel, which results also in a drastical reduction of the drain current. The reduction is much more enhanced for the symmetrical HVMOS case due to the potential drop in the L_{drift} region at the source side. On the contrary the LDMOS device shows gradually increasing current behavior due to the reduction of R_{drift} for increased carrier concentration in the drift region. Thus, it is verified that all specific features of LDMOS/HVMOS devices can be well reproduced with the single model HiSIM-LDMOS/HV. This is an advantage of the modeling based on the surface potential, which additionally secures the consistency of the overall model description.

(a) LDMOS



(b) HVMOS

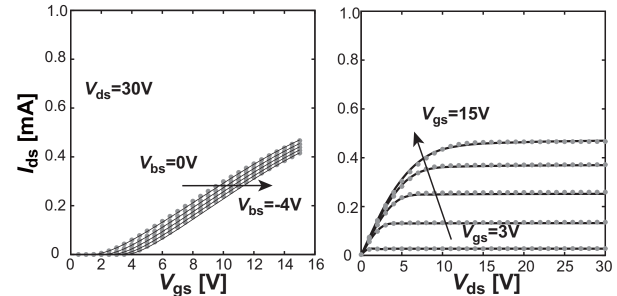


Fig. 8. Current comparison, (left-hand side) as a function of V_{gs} and (right-hand side) as a function of V_{ds}, between LDMOS and HVMOS structures, respectively. Results from HiSIM-LDMOS/HV (lines) and a 2D-device simulator (symbols) are in very good agreement.

Figs. 9a,b compare calculated capacitances for LDMOS and symmetrical HVMOS devices with HiSIM-LDMOS/HV and 2D-device simulation results, respectively. Results agree well for both device structures. The origin for the shoulders in the overall capacitances comes from the overlap capacitances, which are non-negligible for high-voltage MOSFETs.

The scalability of the developed compact high-voltage LDMOS model with the dimensions of the MOSFET part is assured by the application of the surface-potential MOSFET model HiSIM2, which has been verified to accurately reproduce MOSFET properties for all channel length and channel width with a single parameter set [5, 6]. The methodology of HiSIM-LDMOS/HV for consistently determining the potential distribution in MOS channel and drift region furthermore leads to the scaling property with the drift-region length L_{drift}, again with a single model-parameter set for the complete HiSIM-LDMOS/HV model. Fig. 10 verifies these scaling properties with the I_{ds}-V_{gs} characteristics for 3 different L_{drift} values at small and large drain-source bias voltages V_{ds}. It can be seen that the compact model results agree very well with the results of 2D-device simulation at different L_{drift} values.

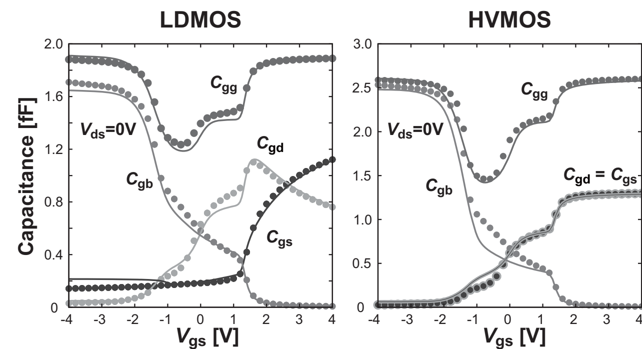


Fig. 9. Comparison of capacitances calculated for the LDMOS and symmetrical HVMOS structures with HiSIM-LDMOS/HV (lines) and a 2D-device simulator (symbols). Again HiSIM-LDMOS/HV is verified to be in good agreement with 2D-device simulation.

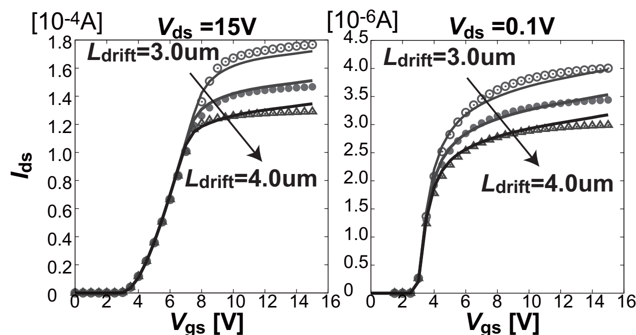


Fig. 10. Scalability of the developed compact high-voltage HiSIM-LDMOS/HV model with drift-region length L_{drift}. The plots show the I_{ds}-V_{gs} characteristics at high and low drain bias in a comparison of 2D-device simulation (symbols) and compact model (lines) results.

5 CONCLUSIONS

We have developed a compact model for high-voltage MOSFETs based on the surface potential distribution in the MOSFET core and its consistent extension to the drift region. The model solves the entire LDMOS/HV structure without relying on any form of macro or subcircuit formulation, accurately reproducing all structure-dependent LDMOS/HV features.

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