Comparison of Four-Terminal DG MOSFET Compact Model with Thin Si Channel FinFET Devices

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ABSTRACT

We discuss a compact model for four-terminal double-gate (DG) MOSFETs based on double charge-sheet drift-diffusion transport, with carrier-velocity saturation. In this model, large V_D at the saturation region is attributed to the infiltrated drain electric field. The latter overrides the drift-diffusion model at the transition point where the quasi-Fermi level is smoothly connected. The model can handle asymmetric gate structure, as well as independent gate voltage for two gates. This approach provides physics-based carrier profile. Comparison with the result of 2D device simulator shows that accurate intrinsic capacitance model has been obtained by the analytical derivative of channel carrier with respect to the terminal voltages. The model was compared with the FinFET samples fabricated by using lightly doped p-type (110) SOI wafers. By fitting five geometrical factors, two flat-band voltages, four transport-related parameters, two extrinsic resistances, the model gives a quite acceptable device model.

Keywords: Compact model, MOSFET, Double-gate, FinFET

1 INTRODUCTION

Ever since the gate length of MOSFET approached 1μm, short channel effect (SCE) has been an annoying problem for device developers. A lot of methods have been introduced to avoid SCE and to keep the pace of design-rule reduction unhindered. Today, exhaustion of such counter-measures is again discussed. To significantly suppress SCE, double-gate (DG) MOSFET structure was proposed [1]. The structure has long been overlooked mainly because of its difficulty for manufacturing. But as the new approach to suppress SCE becomes an imminent issue, the FinFET, which is one of double-gate structures, has gained much attention.

Today, development of new device structures should go with development of its compact model. We proposed a compact model of the DG MOSFET [2]. The model can handle asymmetric gate-structure and four-terminal operation. A new drift-diffusion transport equation was adopted to cope with the carrier-velocity saturation effect directly [3]. The model is now written by Verilog-A, a circuit description language which has recently extended to facilitate subcircuit-style description of the device compact model [4].

In this paper, we first describe present status of the compact model by comparing with the device-simulator results. We then discuss on the comparison with fabricated devices.

2 MODEL

2.1 Transport Equation

As a start point, we assume undoped Si-channel DG MOSFET. Gradual channel approximation and charge-sheet approximation are adopted. Since there are two Si/oxide interfaces, we assume double charge-sheet when perpendicular electric field has a zero-point inside the channel. The absence of space-charge ions means there is linear relationship between i-th charge-sheet carrier densities n_i and the surface potential ψ_j for j-th interface as

$$\psi_j(x) = \sum_{i=1,2} A_{ij} n_i(x) + \text{const}_j \,. \tag{1}$$

By introducing several approximations to decouple two charge-sheets [5], we get the following equation:

$$\psi_i(x) = (q/C_i) n_i(x) + \text{const} \,, \tag{2}$$

where C_i is an effective capacitance.

At high longitudinal electric field $E_{//}$, carrier velocity saturates. This is often expressed as the decrease of carrier mobility μ. In the case of electrons, the replacement of mobility with the following form gives good result.

$$\mu = \mu_S \Big/ \sqrt{1 + \left(\frac{E_{//}(y)}{v_{sat}/\mu_S} \right)^2} \tag{3}$$

where μ_S is the surface mobility, v_{sat} is the saturation velocity. Although μ_S is a function of position y along the

channel, its variation is not large, and here we neglect it. On the other hand, $E_{//}$ dependence of the mobility should be included to treat carrier-velocity saturation rigorously. The resultant transport equation is as follows:

$$-q\mu_S\left(\frac{q}{C}\frac{dn}{dy}n+\frac{kT}{q}\frac{dn}{dy}\right)=I\sqrt{1+\left(\frac{E_{//}}{v_{sat}/\mu_S}\right)^2}\ . \qquad (4)$$

The solution gives the relation between channel length L and carrier density as:

$$L=F(n_a(L))-F(n_a(0))\,, \qquad (5)$$

$$F(n_a(y))=\frac{{n_b}^2\log(n_a+\sqrt{{n_a}^2-{n_b}^2})-n_a\sqrt{{n_a}^2-{n_b}^2}}{2\beta(v_{sat}/\mu_S)n_b}\,, \qquad (6)$$

where $n_a=n/n_{th}+1$, $n_a=(I/qv_{sat})/n_{th}$, and $n_{th}=C/q\beta$.

2.2 Transition Point

In real devices, carrier density at the source and the drain is equal to the doping density N_D. Consequently, carrier density of the charge-sheet at the source/drain end should be n_D, which is the 2D-equivalent of N_D. Therefore, the next step that should be done is to embed the above transport-controlled region within the channel. The widely accepted approach is to set three regions inside the channel [6].

Region I: where carrier density decreases from n_D to $n(0)$, forming the built-in potential barrier. Change in quasi-Fermi level is negligible. Thickness is ignored.

Region II: where the transport equation dominates. The carrier density changes from $n(0)$ to $n(L)$.

Region III: where carrier density increases from $n(L)$ to n_D. Change in quasi-Fermi level is negligible. Thickness is often changed to vary the *effective* channel length.

The drain voltage V_D is then expressed as

$$V_D=\psi(L)-\psi(0)+\beta^{-1}\log(n(0)/n(L))\ . \qquad (7)$$

Although this approach works rather well, it requires arbitrarily small $n(L)$ to produce large V_D. This feature is unacceptable for the velocity-saturation model, because limited carrier velocity implies lower limit of carrier density for a given drain current.

In real devices, such a situation is avoided by a so-called pinch-off condition. When larger drain voltage is applied, the drain electric field, in stead of the lateral electric field formed by the carrier density gradient, start to drag the carriers.

In our model, another region IIb is placed between region II and III, where the drain electric field drags the carrier, and where carrier density is assumed to be constant. The boundary between region II and IIb is defined as a point where the first and the second derivative of the quasi-Fermi level match for both sides. Since the thickness of region IIb expresses channel length modulation effect, thickness of region III is now neglected.

The drain electric field can be assumed to decay exponentially in the channel with the characteristic length λ [7]. If we ignore k-difference between silicon and the oxide, $\lambda=(T_{OX1}+T_{OX2}+T_{Si})/\pi$.

2.3 DIBL

DIBL in DG MOSFETs has similar property to that in SOI MOSFETs, where DIBL is caused by exponentially decaying source/drain electric field [8]. We modeled that the surface potential changes as

$$\Delta\psi(x)=\Delta\psi_S(x)\exp(-x/\lambda)+\Delta\psi_D(x)\exp((x-L)/\lambda) \qquad (8)$$

where $\Delta\psi_S$ ($\Delta\psi_D$) is the potential difference between the surface potential without channel carrier and the source/drain potential. The minimum barrier lowering $\Delta\psi_{MIN}$ gives the DIBL. Although the position for $\Delta\psi_{MIN}$ is away from the source, it is assumed to be the source end.

3 COMPARISON WITH SIMULATOR

3.1 Drain Currents

The comparison with the ATLAS device simulator was made to assure the accuracy of the model. The model parameters were fit to get good agreements both for long and ultra-short channel. Figure 1 shows the comparison of the simulator and the model at L_G=1μm device. Although the matching is good, the model gives lower drain current in some gate1 voltages. Discrepancy may come from different mobility modeling implementation.

The adopted mobility model is remotely related to the CVT model. It includes phonon and surface-roughness mobility as functions of average perpendicular field $E_{\perp av}$.

$$\mu_S^{-1}=\mu_0^{-1}+\left(A_{PH}E_{\perp eff}^{-1/3}\right)^{-1}+\left(A_{SR}E_{\perp eff}^{-2}\right)^{-1} \qquad (9)$$

$$E_{\perp eff}=\sqrt{{E_{\perp av}}^2+(kT/qT_{Si})^2}$$

While this mobility is a function of y in the charge sheet, it is not the function of x (which is the distance from the interface), which is the same as the experimentally extracted mobility. The CVT mobility for the device simulator, on the other hand, is often the function of both x and y. These two implementations result in different models [9]. The difference of these two approaches is exacerbated that the strength of perpendicular electric field in the DG MOSFET channel ranges from zero to a finite value. The necessity of a modified mobility model will be clarified only with the comparison of the compact model to

a long-channel, real device. Since the sample to be used in this paper is ultra-short channel device, little will be known about the adequacy of the mobility model.

Figure 2 shows the comparison with the simulator for ultra-short (30nm) channel structure. In the device, carrier-velocity saturation plays significant role, and discrepancy in the mobility model becomes not prominent.

3.2 Capacitances

Since our compact model incorporates carrier-velocity saturation effect in the transport equation, obtained carrier profile is expected much closer to the real device. Consequently, a good intrinsic capacitance model is expected simply by dedifferentiating gate charges and source/drain charges.

Figure 3 shows the analytically calculated capacitances for a short channel (200nm) device. Since the model does not yet includes fringe capacitances, deviation from the device simulator results are observed in gate-OFF condition. Beside this feature, agreements are excellent in spite of no additional fitting parameter for capacitance modeling.

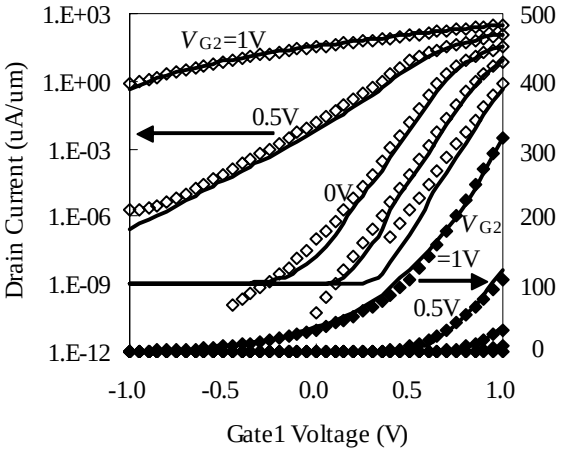


Figure 1: Simulator (marks) and model (lines) results of long (1μm) channel DG MOSFET. Leak current in the model is limited by Gmin.

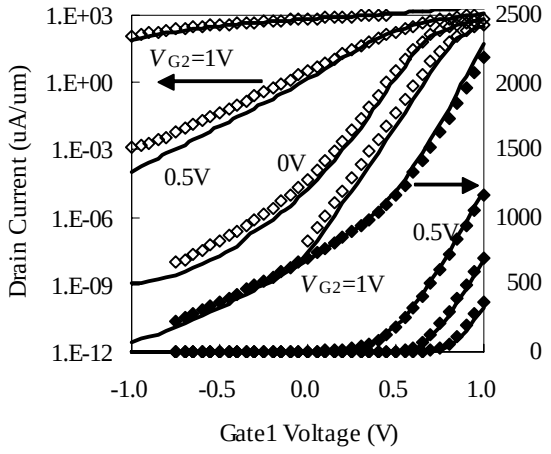
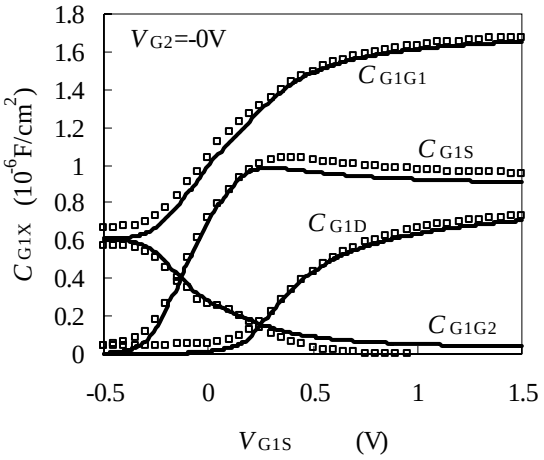


Figure 2: Simulator (marks) and model (lines) results of short (30nm) channel DG MOSFET.

4 COMPARISON WITH REAL DEVICES

FinFET-style DG MOSFETs were fabricated by using lightly doped p-type (110) SOI wafers with 300-nm thick buried oxide layer. To obtain flat interfaces, the Si-channel was formed by anisotropic wet etching process using a tetramethylammonium hydroxide (TMAH) solution. As a result, (111)-oriented, atomically flat surfaces are formed on both sides of a silicon fin structure. The physical gate length L_G was 105nm and the channel thickness T_{Si} was 13nm.



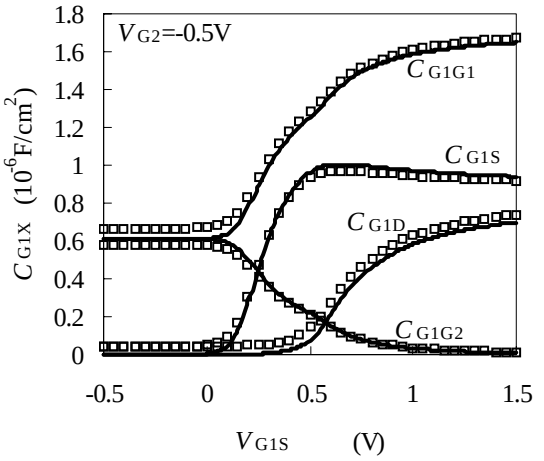


Figure 3: Intrinsic capacitances of four-terminal DG MOSFET. Solid curves are for the model, marks are for the simulator. For both figures, gate length is 200nm, oxide thickness is 2nm, silicon channel thickness is 5nm.

The best fit value for the electrical channel length was 65 nm for the simulator with abrupt source/drain doping and 55nm for the compact model. The difference indicates the definition of channel length in the presence of inevitable doping profile changes slightly between these two methods. The source/drain resistance was 230 Ωμm; a rather reasonable value considering the fabrication process.

No fitting effort was necessary for the channel thickness T_{Si} and oxide *k*. Oxide thickness was slightly (0.4nm) thinned from the measured value (3.2nm). Other parameters were the gate flat-band voltage, the bulk (111)-orientation surface mobility (715.5cm^2/Vs), saturation velocity (1.18x10^{7}cm/s), and three factors to tune the strength of phonon scattering, surface-roughness scattering and DIBL. These are the exhaustive list of fitting parameters.

Figure 3 shows the comparison of I_D-V_G curve. Solid lines are for model results, and the marks are for experimental data. The model is in good agreement except the absence of GIDL current in the model. To get the best fitting for the sample V_{th} roll-off caused by the DIBL is 20% increased compared to the theoretical value.

Figure 4 shows the comparison of I_D-V_D curve. Again, solid lines are for model results, and the marks are for experimental data. Agreement is still rather good considering the small number of fitting parameters.

5 SUMMARY

A compact model for four-terminal double-gate MOSFETs based on double charge-sheet model has been discussed. The basic equations have been explained. The transport equation accommodates carrier velocity saturation explicitly. Comparison with 2D device simulator shows that accurate intrinsic capacitance model has been obtained simply by the analytical derivative of channel carrier with respect to the terminal voltage. Comparison between the model and the data from the fabricated FinFET devices has been in good agreement. Best fit channel lengths for the simulator and the compact model have been similar.

REFERENCES

[1] T. Sekigawa and Y. Hayashi, *Solid-State Electron.*, Vol. 27, pp. 827-828, 1984.

[2] T. Nakagawa, T. Sekigawa, T. Tsutsumi, E. Suzuki, and H. Koike, *Tech. Digest Nanotech 2003*, Vol. 2, pp. 330-333, 2003.

[3] T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki and H. Koike, *Tech. Proc., WCM 2005*, pp. 183-186, 2005.

[4] T. Nakagawa, T. Sekigawa, M. Hioki, S. O'uchi, T. Tsutsumi, and H. Koike, *Tech. Digest IWCM'08*, pp. 17-23, 2008.

[5] T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki, and H. Koike, *Tech. Digest Nanotech 2004*, Vol. 2, pp. 159-162, 2004.

[6] J. R. Brews, *Solid-State Electron.*, Vol. 21, pp. 345-355, 1978.

[7] D. J. Frank, Y. Taur, and H-S. P. Wong, *IEEE Electron Dev. Letts.*, Vol. 19, 1998.

[8] R-H. Yan, A. Ourmazd, and K. F. Lee, *IEEE Trans. Electron Dev.*, Vol. 39, pp. 1704-1710.

[9] H. Shin, A. F. Tasch, C. M. Maziar, and S. K. Banerjee, *IEEE Trans. Electron Dev.*, Vol. 36, pp. 1117-1124, 1989.

[10] Y.X. Liu, K. Ishii, T. Tsutsumi, M. Masahara, and E. Suzuki Y.X. Liu et al., *IEEE Electron Dev. Letts.*, Vol. 24, pp. 484-486, 2003.

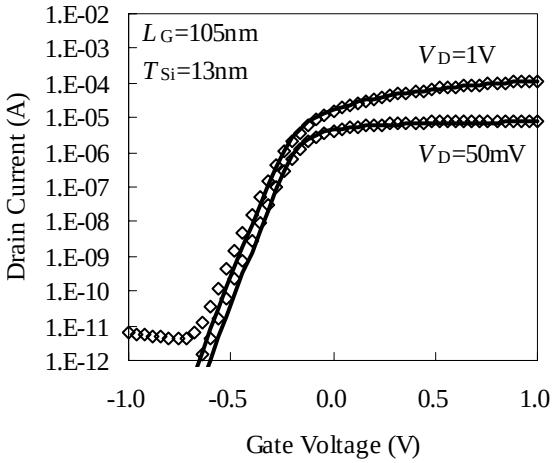


Figure 4: I_D-V_G characteristics of the SOI FinFET (marks) and the model (solid lines).

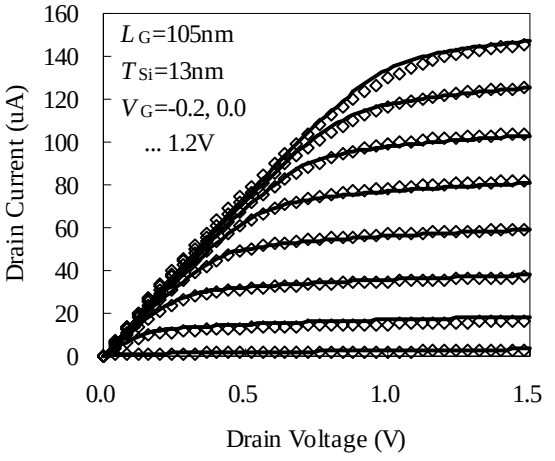


Figure 5: I_D-V_D characteristics of the SOI FinFET (marks) and the model (solid lines).