Capacitance Modeling of Short-Channel DG and GAA MOSFETs

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ABSTRACT

Modeling of the intrinsic capacitances of short-channel, nanoscale DG and GAA MOSFETs is presented, covering a wide range of operation from subthreshold to strong inversion. In subthreshold, the electrostatics is dominated by the inter-electrode capacitive coupling, from which analytical expressions for the charge conserving trans- and self-capacitances of the DG device can readily be derived. Near and above threshold, the influence of the electronic charge is taken into account in a precise, self-consistent manner by combining suitable model expressions with Poisson's equation in the device body. The models are verified by comparison with numerical device simulations.

Keywords: short-channel MOSFET, double-gate, gate-all-around, nanoscale, capacitances, conformal mapping.

1 INTRODUCTION

We have previously presented precise models for the electrostatics and the drain current of short-channel, nanoscale double-gate (DG) and gate-all-around (GAA) MOSFETs [1-7]. These models are based on a procedure where the inter-electrode capacitive coupling between the source, drain, and gates is considered separately as the solution of the Laplace equation for the device body potential. Using conformal mapping techniques, this leads to a precise analytical solution in terms of elliptic integrals for the 2D case of the DG MOSFET [2-4]. We have also shown that the DG results can be successfully applied to the GAA MOSFET by performing an appropriate device scaling to compensate for the difference in gate control between the two devices [6]. These solutions are dominant in subthreshold for low-doped, nanoscale devices.

Near and above threshold, the influence of the electronic charge on the electrostatics is taken into account in a precise, self-consistent manner by combining suitable model expressions with Poisson's equation [7].

Here, we discuss how to derive the intrinsic device capacitances by considering the total, vertical electric displacement field on the gate, source, drain and electrodes from the device electrostatics.

The DG and GAA devices considered have gate length L = 25 nm, silicon substrate thickness/diameter t_{si} = 12 nm, insulator thickness t_{ox} = 1.6 nm, and insulator relative dielectric constant ε_{ox} = 7. The doping density of the *p*-type silicon body is $1\text{x}10^{15}\text{cm}^{-3}$. As gate material, we selected a near-midgap metal with the work function 4.53 eV. Idealized Schottky contacts with a work function of 4.17 eV (corresponding to that of *n*+ silicon) are assumed for the source and drain. This ensures equipotential surfaces on all the device contacts. To simplify the modeling, we replace the insulator by an electrostatically equivalent silicon layer with thickness of $t'_{ox} = t_{ox}\varepsilon_{si}/\varepsilon_{ox}$, where ε_{si} is the relative permittivity of silicon. The device dimensions considered are such that a classical treatment of the electron distribution is warranted.

The modeled capacitances are verified against numerical simulations. Since no fitting parameters are used, the capacitance model together with the corresponding drain current model is scalable over a wide range of geometric and material combinations.

2 ELECTROSTATICS

2.1 Subthreshold

The capacitive coupling between the electrodes of the DG MOSFET is given by Laplace's equation, which can be solved by the technique of conformal mapping [3,4]. The extended four-corner device body of the (*x*,*y*)-plane is mapped into the upper half of a complex (*u*,*iv*)-plane, as indicated in Fig. 1.

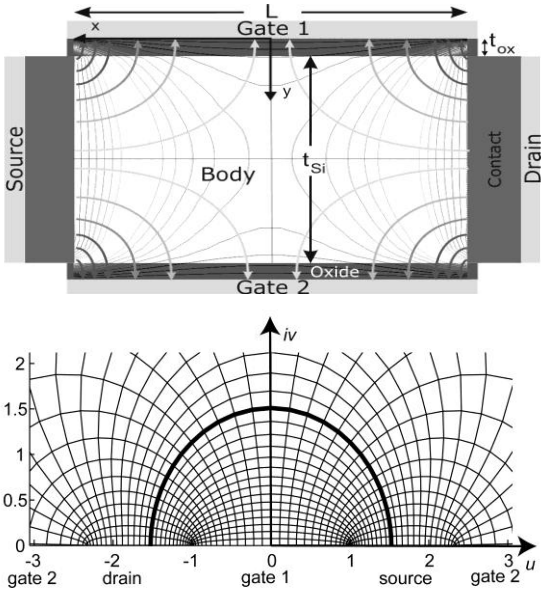


Figure 1: Schematic view of the mapping of a DG MOSFET body (top) into the upper half-plane of the (*u*,*iv*)-plane (bottom). A rectangular grid in the (*x*,*y*)-plane transforms into the grid shown in the (*u*,*iv*)-plane.

The mapping between the two planes is given by the following Schwartz-Christoffel coordinate transformation [3,8]

$$z = x + iy = \frac{L}{2}\frac{F(k,w)}{K(k)} \tag{1}$$

where $w = u+iv$, $F(k,w)$ is the elliptic integral of the first kind, $K(k) = F(k,1)$ is the corresponding complete elliptic integral, and the modulus k is a constant between 0 and 1 determined by the geometric ratio $L/(t_{si} + 2t'_{ox})$. We note that the boundary of the extended, rectangular body in Fig. 1a maps into the real u-axis of the (u,iv)-plane and the four corners map into the position $u = \pm 1$ and $u = \pm 1/k$. Moreover, the vertical imaginary v-axis correspond to the gate-to-gate symmetry axis while the bold semicircle (with the radius $1/\sqrt{k}$) corresponds to the source-to-drain symmetry axis [3].

In the (u,iv)-plane, the inter-electrode contribution to the potential distribution is determined from the Laplace equation as follows

$$\varphi_{DG}^{LP}(u,v) = \frac{v}{\pi}\int_{-\infty}^{\infty}\frac{\varphi_{DG}^{b}(u')}{(u-u')^2+v^2}du' \tag{2}$$

where $\varphi_{DG}^{b}(u')$ is the electrostatic potential along the entire boundary, i.e., along the equipotential surfaces of the source the drain, and the gates, and with minor contributions from the insulator gaps in the four corners. The major terms, corresponding to the case of a very thin insulator, can be expressed analytically in terms of the coordinates u and v [2-5]. The minor terms, which are especially important for determining the capacitances, can be obtained by carefully modeling the potential distribution across the insulator gaps. For this, we apply another conformal mapping procedure suitable for a single corner structure [8], as indicated in Fig. 2. The equipotential lines and the field lines shown for the vicinity of the gap are solutions obtained from this procedure [9]. The bold, dashed line shows the section of the device boundary associated with a single insulator gap. The potential distribution obtained along this line shown in the inset can be approximated by a polynomial of the form

$$\varphi_{ox}(0, y_{1c}) \approx a y_{1c}^{6} + b y_{1c} + V_{gs} - V_{FB} \tag{3}$$

where the parameters a and b are determined from the potential at source or drain, V_{gs} is the gate-source voltage, V_{FB} is the flat-band voltage of the gate, and y_{1c} is the local coordinate along the boundary in Fig. 2.

The GAA MOSFETs are 3D structures that cannot be analyzed the same way. However, because of the cylindrical symmetry, we observe that many structural similarities exist between the 2D potential distribution obtained for the DG MOSFET and that of a longitudinal cross-section through the axis of the GAA device.

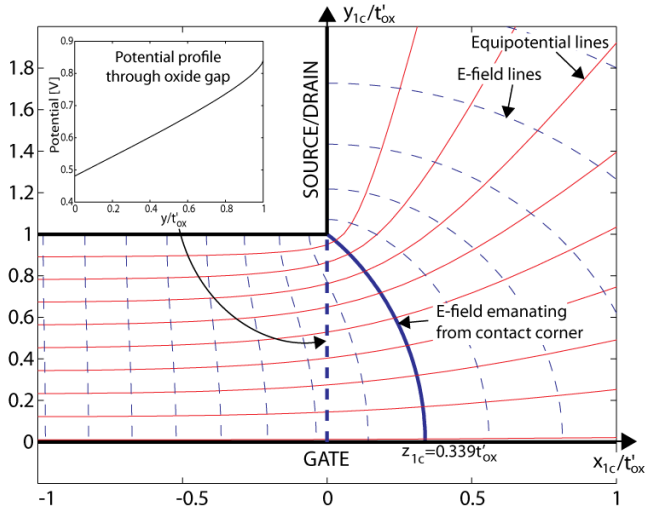


Figure 2: Equipotential lines and field lines from the one-corner analysis with inset showing the potential profile along the boundary through the insulator gap (bold dashed line).

In fact, the major difference between the two is the strength of the gate control. This difference can be expressed in terms of the so-called characteristic lengths, which are a measure of the penetration depth of the contact electrostatic influence along the source-to-drain symmetry axis. The characteristic lengths λ_{DG} and λ_{GAA} for the DG and GAA MOSFETs, respectively, only depend on the silicon and insulator thicknesses and the ratio of their dielectric constants [10,11].

Based on this observation, we propose to approximate the inter-electrode potential distribution of the GAA MOSFET as follows [6]: First we calculate the potential distribution φ_{DG}^{LP} of a DG device with an expanded length $L_{DG} = L\lambda_{DG}/\lambda_{GAA}$, where L is the true length of the GAA device. Next, this potential distribution is compressed uniformly in the longitudinal direction using the scaling factor $\lambda_{GAA}/\lambda_{DG}$ as indicated in Fig. 3. Finally, the resulting distribution is mapped into the central, longitudinal cross-section of the GAA MOSFET.

We emphasize that this procedure for deriving the DG MOSFET inter-electrode potential does not give an exact solution of the 3D Laplace equation for the GAA MOSFET. However, comparisons with numerical calculations show that the error is at most a few millivolts, mostly localized to regions near source and drain.

2.2 Self-consistency

Near and above threshold, the contribution to the body potential from the inversion charge must be included. In this case, Poisson's equation is divided into two superimposed parts, the first of which is the Laplace equation, which describes the inter-electrode capacitive

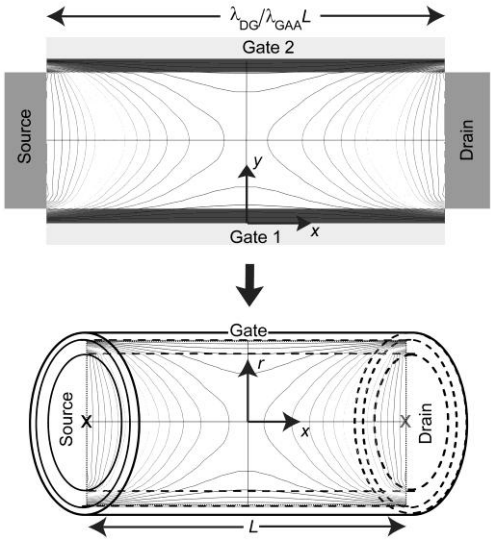


Figure 3: Schematic illustration of the mapping of a DG MOSFET inter-electrode potential distribution for an extended device of length L_{DG} (top) into the longitudinal cross-section of a GAA device of length L (bottom).

coupling discussed in Section 2.1. The second part accounts for the electrostatic effects associated with the charge carriers, which must be derived in a self-consistent manner. With a finite drain bias, the self-consistency also encompasses the quasi-Fermi potential distribution and the drain current.

The self-consistent procedure for modeling the electrostatics and the drain current of both the DG and GAA MOSFETs is described elsewhere [6,7].

3 CAPACITANCE MODELING

From the device electrostatics, it is possible to find the vertical displacement field distributions at the source, drain, and gate electrode surfaces. According to Gauss' law, these fields determine the charges on the electrodes, from which the intrinsic capacitances can be derived.

Taking proper account of all charges, the four-terminal DG MOSFET can be described in terms of 16 trans- and self-capacitances C_{XY}, of which 9 are independent owing to the principle of charge conservation [12]. Here, C_{XY} reflects the change of charge assigned to electrode X for a small variation in voltage applied to terminal Y according to the definition:

$$C_{XY} = \pm \frac{\partial Q_X}{\partial V_Y} \tag{4}$$

where the + sign is used for $X = Y$ (self-capacitances), and the – sign is used for $X \neq Y$ (trans-capacitances). The GAA MOSFET is a tree-terminal device and so is the DG when applying symmetric gate biasing. For this case, the number of capacitances reduces to 9 of which 4 are independent. The equivalent circuit of the three-terminal device is shown in Fig. 4 [13].

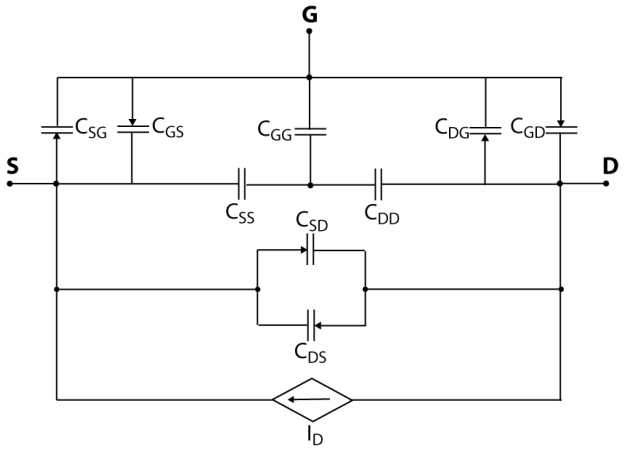


Figure 4: Intrinsic equivalent circuit with charge conserving capacitances for three-terminal MOSFETs.

3.1 Subthreshold capacitances

In subthreshold, the intrinsic capacitances are dominated by the inter-electrode capacitive coupling discussed in Section 2.1. From the major term in (2) (limit of small insulator gaps), we obtain the following expression for the charge on the various electrodes of the DG MOSFET [9]:

$$Q_X = \varepsilon_{si} \int_{z_{min}}^{z_{max}} E_\perp dz = i\varepsilon_{si} \int_{u_{min}}^{u_{max}} \left. \frac{\partial \varphi_{DG}^{LP}}{\partial v} \right|_{v\to 0} du \tag{5}$$
$$= \frac{i\varepsilon_{si}}{\pi} \left[V_G \ln\left(\frac{(u-1)(ku+1)}{(u+1)(ku-1)} \right) + V_S \ln\left(\frac{u+1}{ku+1} \right) + V_D \ln\left(\frac{u-1}{ku-1} \right) \right] \Bigg|_{u_{min}}^{u_{max}}$$

Here, $V_G = V_{gs} - V_{FB}$, $V_S = V_{bi}$, $V_D = V_{ds} + V_{bi}$, where V_{bi} is the built-in voltage of the source and drain contacts and V_{ds} is the drain-source voltage. The limits of integration are the appropriate dimensions of the electrodes over which the intrinsic charges are distributed. For the drain and source electrodes, the integration runs from $y = t'_{ox}$ to $t_{si} + t'_{ox}$ for $x = L/2$ (source) or $x = -L/2$ (drain), or between the corresponding coordinates on the u-axis in the (u, v)-plane. The latter are obtained from the transformation in (1). For the gate electrodes, we notice from Fig. 2 that the charges close to the corners, between the bold solid and dashed lines, correspond to field lines that terminate on the sides of the source/drain electrodes. Therefore, in order to preserve intrinsic total charge neutrality, these charges should be excluded and assigned to the extrinsic capacitances. From the one-corner analysis, we find that the integration for the intrinsic gate charge should run between $x = -L/2 + x_0$ and $L/2 - x_0$ for the two gates, where $x_0 = 0.339t'_{ox}$, or between the corresponding coordinates along the u-axis in the (u,iv)-plane.

Analytical expressions for the subthreshold capacitances are obtained by introducing (5) in (4). We

note that since (5) is linear in the applied voltages, these capacitances are voltage independent. However, in order to improve the precision, we should also include the corrections in the electrostatics associated with the finite insulator thickness (see Section 2.1). This is done by applying (3) in (2) to correct Q_X in (5). The adjusted capacitances are used when comparing the model with numerical simulations below.

The modeling of the subthreshold capacitances in the GAA MOSFET follows the same procedure as outlined above for the DG MOSFET, but with a proper account for the cylindrical symmetry of the GAA device.

3.2 Self-consistent capacitances

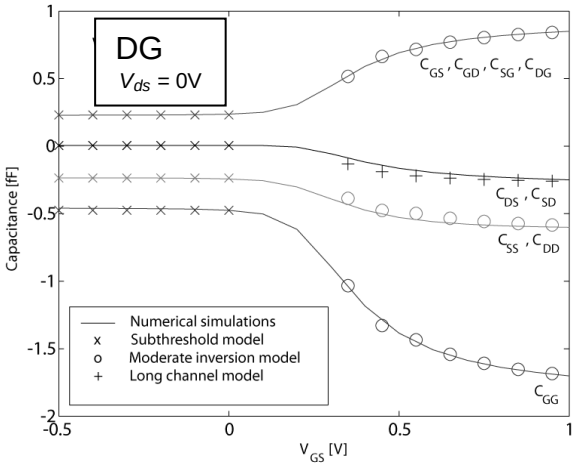
From near threshold to strong inversion, the effect of the inversion charges on intrinsic device capacitances will steadily increase in importance. From the self-consistent device electrostatics in this regime, we again find the perpendicular electric field on the electrodes, from which the total electrode charges Q_S, Q_D, and Q_G and the intrinsic capacitances are determined. However, especially the mirror charges Q_{Sc} and Q_{Dc} owing to the body inversion charge Q_{Bc} may be difficult to determine precisely this way because of strong corner effects.

An alternative procedure is therefore to calculate Q_{Bc} in addition to Q_G and determine the mirror charge on the gate as $Q_{Gc} = Q_G - Q_{Gi}$, where Q_{Gi} is the contribution from the inter-electrode coupling (see Section 3.1). Hence, from charge conservation we have $Q_{Sc} + Q_{Dc} = -(Q_{Bc} + Q_{Gc})$. At zero drain-source bias, this simplifies to $Q_{Sc0} = Q_{Dc0} = -(Q_{Bc0} + Q_{Gc0})/2$.

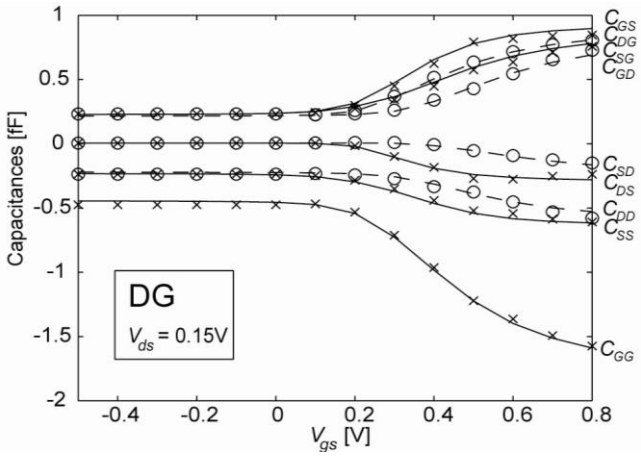
With applied drain-source bias, we can approximate Q_{Sc} and Q_{Dc} quite well by requiring overall charge neutrality between the body charge and its mirror charges in the source-side half and in the drain-side half of the device separately. To find the total charges, we have to include the contributions from the inter-electrode coupling.

Based on the above analysis, we again obtain the self-consistent, intrinsic capacitances from (4). However, we note that well above threshold, the inversion charge contribution to the body potential will be dominant and the electrons tend to screen out the effects of the inter-electrode capacitive coupling except for the regions close to source and drain. Hence, the device electrostatics and the capacitances can be modeled according to a simplified strong-inversion, long-channel analysis [14-16].

In Figs. 5 and 6 are shown a comparison of modeled and numerically simulated capacitances versus V_{gs} for the DG MOSFET and the GAA MOSFET, respectively. Two values of the drain bias are used in each case. In all cases, we observe a very satisfactory correspondence between the model and the simulation, considering that no adjustable parameters are used in the modeling.



a)

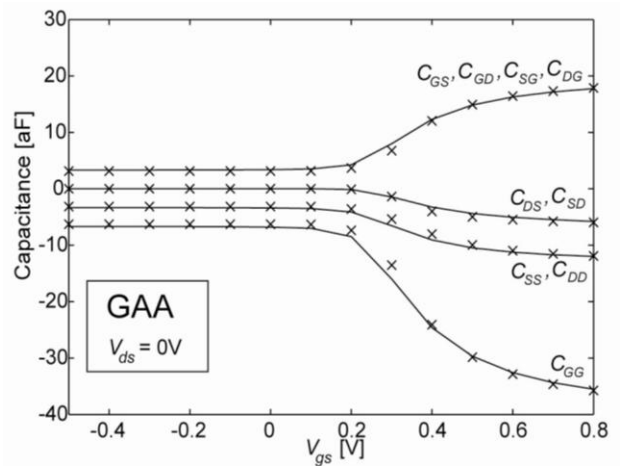


b)

Figure 5: Modeled DG MOSFET capacitances (symbols) for V_{ds}= 0 V (a) and 0.15 V (b). The curves are obtained from numerical simulations using the Silvaco Atlas device simulator.

4 CONCLUSION

We have developed a precise 2D modeling framework for calculating the intrinsic, charge conserving capacitances of nanoscale, short-channel DG and GAA MOSFETs. The 2D modeling is based on conformal mapping techniques and a self-consistent analysis of the device electrostatics that include the effects of both the inter-electrode capacitive coupling between the contacts and the presence of inversion electrons. The modeling framework covers a wide range of bias voltages from subthreshold to strong inversion. The capacitances calculated from the present model show very good agreement with those from numerical simulations (Silvaco Atlas).



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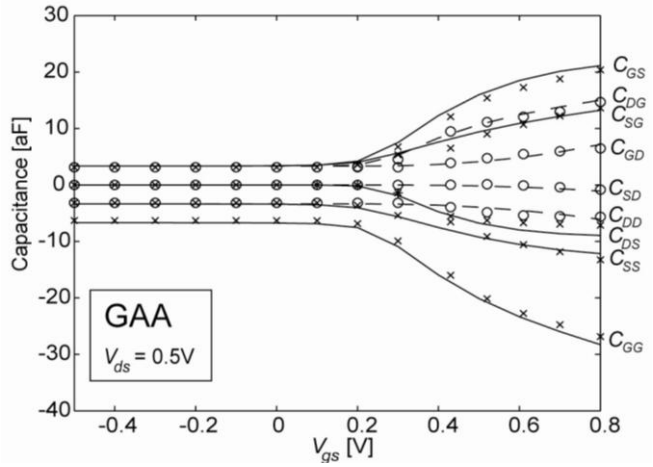

b)

Figure 6: Modeled GAA MOSFET capacitances (symbols) for V_{ds}= 0 V and 0.1 V. The curves are obtained from numerical simulations (Silvaco Atlas).

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