Benchmarking Performance and Physical Limits on Processing Electronic Device and Systems: Solid-State, Molecular and *Natural* Processing Paradigms

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ABSTRACT

This paper examines the physical and technological limits imposed on processing devices which predefine hardware and software solutions. We study various constraints which are imposed. The emerging molecular processing paradigm promises one to ensure benchmarking overall performance in data processing. The soundness of *fluidic* and *solid* solutions is studied. We discuss the use of basic physics, implication of the Heisenberg uncertainty principle, as well as technologies which ultimately may affect various approaches. *Natural* and *engineered* molecular processing solutions are profoundly different. In general, the comparison cannot be made because *natural* processing is not comprehended at the *device* and *system* levels. The information processing, performed by *natural* systems, is a frontier for multidisciplinary research. Therefore, we concentrate on data processing accomplished by *engineered* molecular primitives and platforms. This molecular solution is fundamentally different when compared to solid-state microelectronics due to distinct device physics, system organization, technology, software, etc. The case-studies are reported.

Keywords: electronic device, physical limits, processing

1. INTRODUCTION

For solid-state microelectronics, basic physics and sound fundamentals were largely developed [1, 2]. The established CMOS technology currently progresses to the 45 and 32 nm technology nodes with the expected *effective* field-effect transistor dimensionality ~500×500 nm [3]. However, microelectronics faces many challenges. The major challenges are [1-5]:

1. Fundamental limits at the device, module and system levels are nearly achieved,
2. Stringent technological constraints and affordability rationale emerged and cannot be overcome.

Therefore, sound innovative solutions are sought. *Solid* and *fluidic* molecular processing devices (^{M}devices) and processing platforms (^{M}PPs) were proposed in [6-9]. Molecular processing encompasses novel 3D-topology ^{M}devices, new organization, advanced architecture and *bottom-up* fabrication [9-11].

The *reachable* volumetric dimensionality of *solid* and *fluidic* molecular processing primitives is in the order of 1×1×1 nm. Solid molecular electronic devices (^{ME}device) were studied in [6-9]. For ^{ME}devices, due to synthesis, interface and other constraints, the *achievable equivalent* device cell volumetric dimensionality is expected to be ~10×10×10 nm [9]. These multi-terminal ^{ME}devices can be synthesized and aggregated as ^{N}hypercells forming functional ^{M}ICs. These ^{M}ICs implement complex combinational circuits, processors, memories, etc. [9-11].

New device physics, innovative organization, novel architecture, enabling capabilities and functionality are the key essential features of molecular and nano electronics. Molecular, atomic and subatomic devices, as compared to semiconductor devices, are distinguished by distinct device physics. ^{M}Devices may:

1. Exhibit exclusive phenomena;
2. Ensure exceptional performance;
3. Provide enabling capabilities;
4. Possess unique functionality.

These ^{M}device may typify, to some extent, processing biomolecular primitives of *natural* PPs (^{N}PPs). However, the device physics is fundamentally distinct. Furthermore, ^{N}PPs perform information processing and are not comprised from ^{M}IC or any *circuit* equivalents. As

- *Natural* biomolecular processing primitives will be coherently examined, assessed and evaluated,
- Information processing of ^{N}PPs will be comprehended,

the benchmarking performance quantitative metrics and qualitative measures of *natural* processing (computing) performance and capabilities may be established.

Due to unsolved problems in information processing and *natural* processing, we focus on ^{M}PPs. The combinational and memory ^{M}ICs can be designed as aggregated ^{N}hypercells comprised from ^{M}gates and molecular memory cells. From the system-level consideration, ^{M}ICs can be designed within novel organization and enabling architecture which guarantee superior performance and exceptional capabilities.

2. PHYSICAL LIMITS AND ENERGETICS

We study physical limits and research performance estimates. The designer examines the device and system performance and capabilities using distinct performance measures, estimates, indexes and metrics. At the device level, we examine functionality, study characteristics and estimate performance of 3D-topology ^{M}devices. The experimental results indicate that electrochemomechanical transitions in biomolecules and proteins are performed within 1×10^{-6} to 1×10^{-12} sec, and requires ~1×10^{-19} to 1×10^{-18} J of energy [9].

To analyze protein energetics, examine the switching energy in microelectronic devices, estimate *solid* ^{ME}devices

energetics and perform other studies, distinct concepts are applied. For solid-state microelectronic devices, the logic signal energy is expected to be reduced to $\sim 1\times10^{-16}$ J [3]. The energy dissipated is

$E=Pt=IVt=I^2Rt=Q^2R/t$,

where P is the power dissipation; I and V are the current and voltage along the discharge path; R and Q are the resistance and charge.

The dynamic power dissipation (consumption) in CMOS circuits is analyzed. Using the equivalent power dissipation capacitance C_{pd} (expected to be reduced to $\sim 1\times10^{-12}$ F [3]) and the transition frequency f, the device power dissipation due to output transitions is $P_T=C_{pd}V^2f$. The energy for one transition can be found using the current as a function of the transition time which is found from the equivalent RC models of solid-state transistors. The simplest estimate for the transition time is $-RC\ln(V_{out}/V_{dd})$. During the transition, the voltage across the load capacitance C_L changes by $\pm V$. The total energy used for a single transition is charge Q times the average voltage change, which is $\frac{1}{2}V$. The total energy per transition is $\frac{1}{2}C_{Load}V^2$. If there are $2f$ transitions per second, one has $P_L=C_LV^2f$. Therefore, the dynamic power dissipation P_D is

$P_D=P_T+P_L=C_{pd}V^2f+C_LV^2f=(C_{pd}+C_L)V^2f$.

For ^{M}devices and ^{ME}devices, this analysis cannot be applied. The term k_BT has been used to solve distinct problems. Here, k_B is the Boltzmann constant, $k_B=1.3806\times10^{-23}$ J/K; T is the absolute temperature. The expression γk_BT ($\gamma>0$) was used to assess the energy, and $k_BT\ln(2)$ was applied with the attempt to assess the lowest energy bound for a binary switching. The applicability of distinct equations must be examined applying sound concepts. Statistical mechanics and entropy analysis coherently utilize k_BT and $k_B\ln w$ within a specific content.

By letting $w=2$, the entropy is $S=k_B\ln2=9.57\times10^{-24}$ J/K. Having derived S, one cannot conclude that the minimal energy required to ensure the transition (*switching*) between two *microscopic* states or to erase a bit of information (energy dissipation) is $k_BT\ln2$, which for $T=300$K gives $k_BT\ln2=2.87\times10^{-21}$ J. In fact, under this reasoning, one assumes the validity of the *averaging* kinetic-molecular Newtonian model and applies the assumptions of distribution statistics, at the same time allowing only two distinct *microscopic* system's states.

The energy estimates are performed utilizing quantum mechanics. To examine the discrete energy levels of an electron in the outermost populated shell, one applies

$$E_n=-\frac{m_eZ_{eff}^2e^4}{32\pi^2\varepsilon_0^2\hbar^2n^2},\ \text{and}\ E_n=-2.17\times10^{-18}\frac{Z_{eff}^2}{n^2}\ \text{J}.$$

From $Z_{eff}/n\approx1$, one concludes that ΔE is from $\sim 1\times10^{-19}$ to 1×10^{-18} J. If one supplies the energy greater than E_n to the electron, the energy excess will appear as kinetic energy of the free electron. The transition energy should be adequate to excite electrons. For different atoms and molecules, as the prospective *solid* ^{ME}devices, the transition (switching) energy is estimated to be $\sim 1\times10^{-19}$ to 1×10^{-18} J. This estimate is in agreement with biomolecular devices. The energy of a single photon is $E=hc/\lambda$. The maximum absorbance for rhodopsin is ~500 nm. Hence $E=4\times10^{-19}$ J. This energy is sufficient to ensure transitions and functionality.

Considering an electron as a non-relativistic particle, taking note of $E=\frac{1}{2}mv^2$, we obtain the particle velocity as a function of energy, and $v(E)=\sqrt{\frac{2E}{m}}$.

For $E=1.6\times10^{-20}$ J, one finds $v=1.9\times10^{5}$ m/sec.

Assuming 1 nm path length, the traversal (*transit*) time is $\tau=L/v=5.3\times10^{-15}$ sec. Hence, ^{ME}devices can operate at a high switching frequency. However, one may not conclude that the device switching frequency to be utilized is $f=1/(2\pi\tau)$ due to device physics features (number of electrons, heating, interference, potential, energy, noise, etc.), system-level functionality, circuit specifications, etc.

Natural, biomolecular, *fluidic* and *solid* devices and systems exhibit distinct performance and capabilities. The advancements are envisioned towards *solid* molecular electronics typifying ^{N}PPs. One can resemble a familiar solid-state microelectronics solution. *Solid* ^{ME}devices and ^{M}ICs may utilize the *soft materials* such as polymers and biomolecules. Figure 1 reports some performance estimates. Here, a neuron is represented as a *natural* information processing/memory module (system) [9].

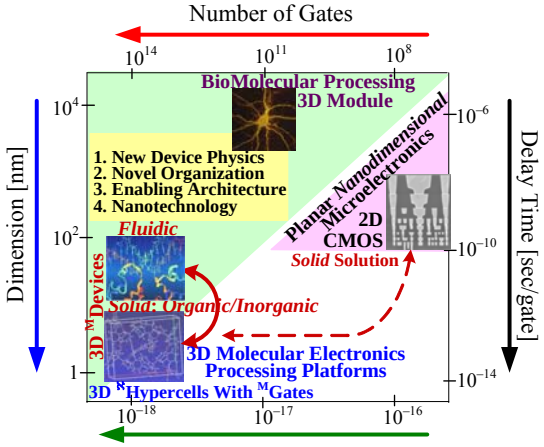


Figure 1. Towards molecular electronics and processing/memory.

Revolutionary advancements:

1. From data processing to information processing frontiers;
2. From 2D microelectronics to 3D molecular electronics;
3. From ICs to ^{M}ICs, and to ^{M}PPs typifying ^{N}PPs;
4. From *bulk* to *bottom-up* synthesis and fabrication.

We studied the *microscopic* system energetics applying quantum mechanics. Though these variations can be utilized by *microscopic* systems ensuring overall functionality and soundness of ^{M}devices, the resulting changes and transitions must be observed and characterized. The device, module and system testing, characterization and evaluation are critical, and PPs cannot be designed without these tasks. The Heisenberg uncertainty principle provides the fundamental limits due on the measurements implying constraints on the testability, characterization, etc.

In particular, the Heisenberg uncertainty principle provides the position-momentum and energy-time limits on the measurements as $\sigma_x\sigma_p \geq \frac{1}{2}\hbar$ and $\sigma_E\sigma_t \geq \frac{1}{2}\hbar$.

Using the energetic estimates, letting σ_E to be 1×10^{-18} J, one obtains $\sigma_t \geq 5\times10^{-15}$ sec. This result complies with the derived *transit* time $\tau=5.3\times10^{-15}$ sec. It should be emphasized, that the Heisenberg uncertainty principle does not define the device functionality and/or physical limits on energy, *transit* time, momentum, velocity, device dimensionality, etc.

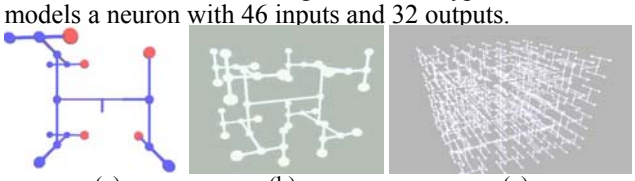
3. Design of Processing Platforms: System Organizations and Architectures

We initiate the studies in the design and software developments for envisioned molecular hardware solutions. These problems are frontiers of electrical and computer engineering, computer science and other disciplines, such as physics, chemistry, biology, neuroscience, mathematics, etc. Enormous research efforts are needed, and our intent is to report possible solutions, propose innovative inroads, and report up-to-date major results.

The analysis and design of ^{M}PPs must be three dimensional, and the third dimension Z carries the functional information, that is, $f=f(X,Y,Z)$. There are several known approaches for computing in 3D. The first approach is based on the idea that the 2D computational structures can by layered and assembled by utilizing 2D layers as $f=f_1(X,Y)\times f_2(X,Y)\times\ldots\times f_k(X,Y)$, where functions f_1, f_2, ..., f_k correspond to the first-, second-, …, k-th levels; × denotes an assembling operation. This approach is used in VLSI and ULSI. The logic network (with a physical implementation as a planar 2D silicon design) is layered and interconnected (between layers) to achieve the desired functionality. The interconnected layers form the "third dimension". In this approach, the "third dimension" does not carry any functional information about the implemented logic functions. This computational 3D concept is not adequate to the *natural*, *engineered* and other molecular solutions. The second approach is based on the mapping of a logic function into a system with "three coordinates" [12]. This approach requires complex transformations of logic functions with respect to each dimension. The main drawback is that the known techniques of logic network design cannot be used in the representation of logic functions in a 3D space. That is, each logic function requires a 3D expansion [13]. This approach is obscure because it requires a complete revision of the previously developed methods, techniques, tools, etc. The third approach is related to the 3D cellular arrays and their particular case, 3D systolic arrays [10, 11]. These structures are very complicated in design and control. Correspondingly, they have not been fully implemented in practice. However, the linear systolic arrays are found to be tractable and practical [10, 11, 14]. They can be used in the 3D computing structure design.

We are developing a novel computing paradigm which can be applied to arbitrary computing platforms, e.g., conventional and envisioned ^{M}PPs. Furthermore, our concept, supported by a set of efficient methods and tools, is expected to be applicable to assess and study *natural* processing. In the proposed approach, several major problems, which have not been solved by the known methods, are successfully resolved [10, 11]. Hence, we overcome the design complexity problem relaxing the *design complexity limits*. Our design complexity for the homogeneous arrays is $kO(n)$, where n is the number of logic variables. In contrast, the application of conventional methods can lead to the complexity $O(n^3)$. In the proposed design, the homogenous and massive parallelism principles are implemented at the device level without loss of the universality of computing. This is very important for the design and analysis of the processing platforms and their implementation using current and prospective solutions.

To date, we have applied advanced analysis and design methods, some of which were reported in [10, 11]. These concepts, supported by a 3D©NeuralNet toolbox which utilizes computationally-efficient algorithms, are developed to attack super-large-scale problems. That is, design of computing feedforward networks of neurons with 1×10^9 to 1×10^{10} connections is potentially possible by further advancing our toolbox. Various computing architectures were designed. Networks can be embedded into 3D structures using H-trees representation in spatial dimensions [11]. We use the established benchmarks to verify and compare the results with conventional design methods. We replaced logic primitives (AND, OR, NAND, NOR and other gates) by a 3D ^{N}hypercube as illustrated in Figures 2.a and b. A node in the decision tree realizes the Shannon expansion $f = \bar{x}_i f_0 \oplus x_i f_1$, where $f_0=f(x_i=0)$ and $f_0=f(x_i=1)$ for all variables in f. The terminal nodes carry information of computing flow. Figure 2.c illustrates a spatial topology neuron network, consisting of 546 ^{N}hypercubes, which models a neuron with 46 inputs and 32 outputs.



(a) (b) (c)

Figure 2. (a) Optimized spatial topology of a 4-input neuron; (b) Aggregated 5-input neuron; (c) 3D representation of a neuron with 46 inputs and 32 outputs generated by 3D©NeuralNet package

We develop and evaluate a decision diagram-based approach which simplifies the connections or the *path* between two arbitrary neurons in 3D. The alternative to the hypercube-based approach is to describe the logic function between neurons by a set of linear decision diagrams [10, 11]. The linear decision diagrams can be directly mapped into *linear arrays*. A 3D©NeuralNet toolbox can generate computing neural structures based on principles of massive parallelism guarantying *array* processing.

A computing array consists of *operational* and *memory* arrays of primitives as reported in Figure 3. The array specificity is defined by the need for functionality- and efficiency-focused design and optimization at the various design and implementation levels. For example, switches, various logic devices, memory, data transmission and other primitives are characterized by different requirements, specifications, performance, capabilities, etc. Our concept perfectly suits molecular, biomolecular and micro technologies. The proposed solution is expected to be applicable to the *natural* processing. The advantage of the proposed array architecture is a straightforward aggregation

of 2D and 3D arrays. This array utilizes specific properties of liner decision diagrams [10, 11]. Table 1 reports the results of our numerical studies. For example, for the sao2 circuit, 3D©NeuralNet generates a 3D 10-input and 4-output neural network with 33 terminal nodes, 100 intermediate (operational) nodes and 133 interconnections.

Table 1. Modeling of 3D feedforward neural networks based on embedding decision diagrams into 3D ^{N}hypercube structures

Benchmarks	# I/O	# Terminal nodes	# Intermediate nodes	# Connections
9sym	9/1	99	298	397
clip	9/5	149	448	597
sao2	10/4	33	100	133

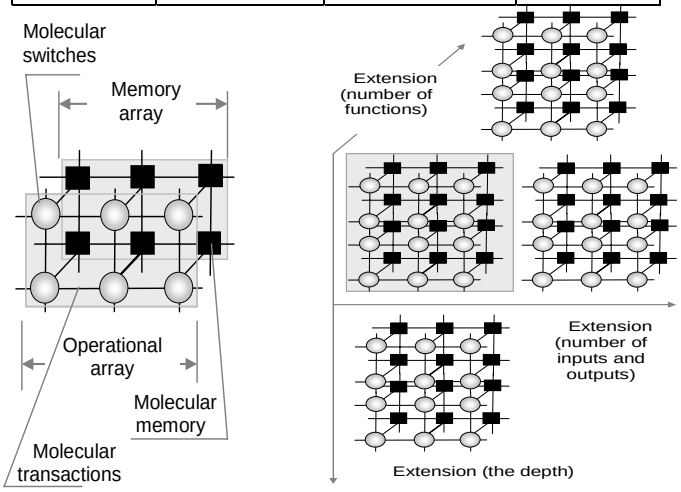


Figure 3. (a) 3D structure composed from linear arrays; (b) Aggregation in 3D space

Our goal is to increase the computational power of 3D neural networks. We represent a neuron by a multiple-valued structure which processes data on radix 3, 4, …,16. A 3D©NeuralNet package can manipulate multiple-valued data structures. A high radix improves performance, capabilities and efficiency of neural networks. We encoded multiple-valued data by binary codes ensuring soundness [10]. The modeling results for the 4-valued neural networks are given in Table 2. In particular, three ICs (c2670 ALU/control, c5315 ALU, and c7552 adder/comparator) are studied. Enhancing information content (quaternary versus binary) does not requires the doubling of computational resources. This result is verified for the 8- and 16-valued data. In our preliminary studies, we did not examine the data reliability which affected by noise, noise/signal ratio and other factors related to data transmission, hardware solutions, functionality, etc.

Table 2. Modeling of 3D neural networks using multiple-valued data structures

TEST	INPUT / OUTPUT	#LEVEL	#CELL	VOLUME
c2670	233/140	40	1374	1375×40×140
c5315	178/123	68	3192	3192×68×123
c7552	207/108	64	4627	4627×64×108

4. CONCLUSIONS

For emerging processing devices and platforms, we derived and reported the physical and technological limits. *Natural* and *engineered* molecular processing solutions were examined at the device and system levels. The results contributed to the design and analysis of *engineered* molecular processing devices and platforms. We studied and reported the fundamental differences between data and information processing in *engineered* and *natural* systems, which are the frontiers of a multidisciplinary research [15]. The applications of novel design methods, supported by the developed software tools, were presented to demonstrate feasibility and practicality in synthesis of ^{M}PPs achieving super-large-scale-integration capabilities.

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