Analytical modelling and performance analysis of Double-Gate MOSFET-based circuit including ballistic/quasi-ballistic effects

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ABSTRACT

In this paper we present a compact model of Double-Gate MOSFET architecture including ballistic and quasi-ballistic transport down to 20 nm channel length. In addition, this original model takes into account short channel effects (SCE/DIBL) by a simple analytical approach. The quasi-ballistic transport description is based on Lundstrom's backscattering coefficient given by the so-called flux method. We also include an original description of scattering of processes by introducing the "dynamical mean free path" formalism. Finally, we implemented our model in a Verilog-A environment, and applied it to the simulation of circuit elements such as CMOS inverters and Ring Oscillators to analyze the impact of ballistic and quasi-ballistic transport on circuit performances.

Keywords: Double-Gate MOSFET, ballistic/quasi-ballistic transport, compact model, Ring Oscillator.

1 INTRODUCTION

As the MOSFET continues to shrink rapidly, emerging physical phenomena, such as ballistic transport, have to be considered in the modelling and simulation of ultra-scaled devices. Future Double-Gate MOSFETs (DGMOS Fig. 1), designed with channel lengths in the decananometer scale, are expected to be more ballistic or quasi-ballistic than diffusive. At this level of miniaturisation is essential to directly evaluate the impact of ballistic and quasi-ballistic transport at circuit level through simulation of several circuit demonstrators. The implementation of compact models in Verilog-A environment offers the opportunity to describe as accurately as possible the physics of transport and to analyze its impact on various circuit elements.

Several analytical models based on the Drift-Diffusion formalism demonstrate that is possible to introduce the diffusive transport in compact modelling. However, when the channel length approaches the value of mean free path, the mobility definition can no more strictly explain the electronic transport in the device. In this case we use the flux theory and the main parameter of this approach is the backscattering coefficient, which expresses the ballistic and the quasi-ballistic transport. Some well-known works performed by Lundstrom *et al* [1-2] demonstrate the usefulness of the flux theory in qualitatively describing quasi-ballistic transport in compact modelling.

In this work we demonstrate the feasibility of a simulation study of ballistic/quasi-ballistic transport at circuit level and we show the impact of this advanced transport on the commutation of CMOS inverter and the oscillation frequency of ring oscillator. This paper is organized as follows: the section I explains the model physics and the corresponding assumptions. In part II, we explain our device simulation in ballistic and quasi-ballistic case. Finally, we highlight the qualitative connection between physics of quasi-ballistic transport and its impact on circuit performance is thoroughly analyzed.

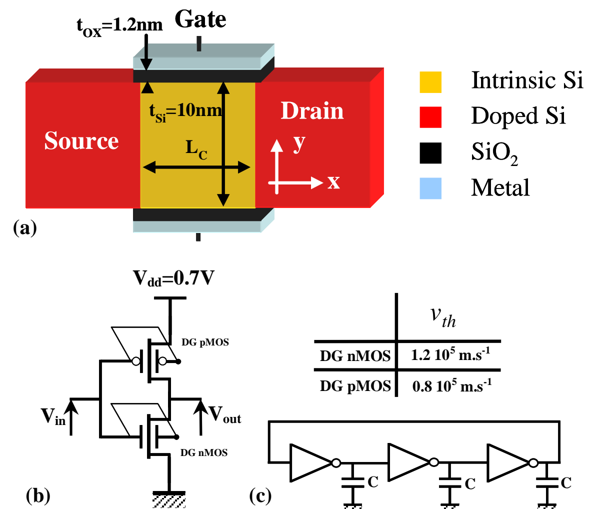

Figure 1: Double-Gate MOSFET (a), CMOS inverter (b), ring oscillator (c) and definition of the main geometrical and electrical parameters.

2 DG MOSFET MODEL

The proposed analytical model (implemented in Verilog-A environment) is based on the well-known work of Natori [3] and Lundstrom [1]. This formula describes the ballistic and quasi-ballistic current:

$$I_D = W.C_{ox}.(V_{GS} - V_T).v_{th}.\left(\frac{1-R}{1-R}\right).\left(\frac{1-e^{-qV_{DS}/k.T}}{1+\left(\frac{1-R}{1-R}\right)e^{-qV_{DS}/k.T}}\right) \quad (1)$$

where W is the gate width, C_{ox} is the gate oxide capacitance, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, V_T is the threshold voltage, k is the Boltzmann constant, q is the electron charge and T is the lattice temperature.

In addition, Lundstrom *et al.* developed physical compact models describing the device operation in quasi-ballistic regimes using the backscattering coefficient R [3]:

$$R = \frac{L_{kT}}{\lambda + L_{kT}} \; ; \; L_{kT} = L_c.\frac{k.T}{q.V_{DS}} \quad (2)$$

where λ is the mean free path and L_{kT} is the distance over which the channel potential drops by kT/q compared to the peak value of the source to channel barrier. Physically, L_{kT} represents the critical distance over which scattering events modify the current; L_{kT} depends on both source-to-drain drop voltage and gate length [2].

We consider here the Dynamical mean Free Path which is a "local free path of ballistic carriers" [4]. This characteristic length represents the average distance to be crossed before the next scattering event. This approach considers that each carrier is ballistic as long as any event does not disturb its trajectory. The dynamic mean free path connects the ballistic velocity and all interactions (coulomb and acoustic/optical phonon interaction) experienced by carriers crossing the channel. The scattering process with impurities (τ_{imp}) and phonon interactions (τ_{ph}) are calculated as in [4] and the value of dfp used here is 27 nm in the intrinsic silicon channel. In practice, *dfp* replaces λ to describe quasi-ballistic transport:

$$dfp = v_{bal}.\tau_{tot} \; ; \begin{cases} \tau_{tot}^{-1} = \tau_{imp}^{-1} + \tau_{ph}^{-1} \\ v_{bal} = \sqrt{\frac{2.\varepsilon_{bal}}{m^*}} \\ \varepsilon_{bal} = \frac{3}{2}.k.T + q.V_{DS} \end{cases} \quad (3)$$

where m^* is the mass in direction of transport, v_{bal} the ballistic velocity, τ_{tot} the total scattering rate and ε_{bal} the carrier energy.

To obtain an accurate model and describe all electrostatic effects, we have also introduced Short Channel Effect and Drain Induced Barrier Lowering (SCE/DIBL) using the Suzuki's model [5] for V_T. Thus, V_T in equation (11) is modified by ΔV_T:

$$V_T = V_{th} - \Delta V_T \quad (4)$$

where V_{th} and ΔV_T are the long channel threshold voltage and its variation due to SCE/DIBL.

The above-threshold regime is linked to the subthreshold regime using an interpolation function based on the subthreshold swing S parameter also defined by Suzuki in [5]. This assures the perfect continuity of our model between on-state current (I_{on}) and off-state current. The definition of V_{th}, ΔV_T and S will be not detail in this paper, but can be found in [5].

3 DEVICE SIMULATIONS

After implementation in Verilog-A environment, the model has been used to simulate the DGMOS structure schematically presented in Figure 1. The source and drain regions are heavily doped (1×10^{20} cm^{-3}) and an intrinsic thin silicon channel is considered. The channel length varies from 10 nm to 200 nm; a gate oxide of 1.2 nm thick and a midgap metal gate are also considered.

It is well-known that the ballistic current is independent of channel length [3] except when SCE or DIBL appears. In order to clearly confirm this point, simulations have been performed for several length (20, 25, 30, 40, 50, 100 and 200 nm) and considering two types of transport (quasi-ballistic and ballistic; Fig. 2). Note that for the ballistic case, the mean free path value has been chosen to be extremely large compared to the channel length. In contrast to the ballistic case, the quasi-ballistic transport has the same behaviour as that of diffusive transport and the form of the output characteristics depends on L_c.

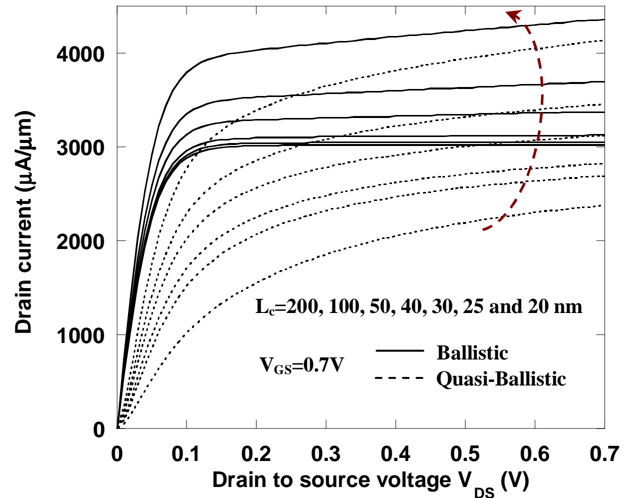

Figure 2: Drain current versus V_{DS} for L_c=200, 100, 50, 40, 30, 25 and 20 nm and V_{GS}.

Figure 3 shows drain current versus the gate voltage characteristics for the DGnMOS and DGpMOS simulated devices at V_{DS}=0.7V. In this approach, we suppose that the transport description (for ballistic and quasi-ballistic case) for holes is identical to that of electrons, with uniquely changing the thermal velocity value in non-degenerate conditions [6]. As expected, the ballistic and quasi-ballistic current shows a perfect continuity between the above and the subthreshold regime (illustrate on Fig. 3a). Finally, figure 3b shows that DGnMOS and DGpMOS have the same behaviour in terms of transport, with different current levels due to the different values of thermal velocity.

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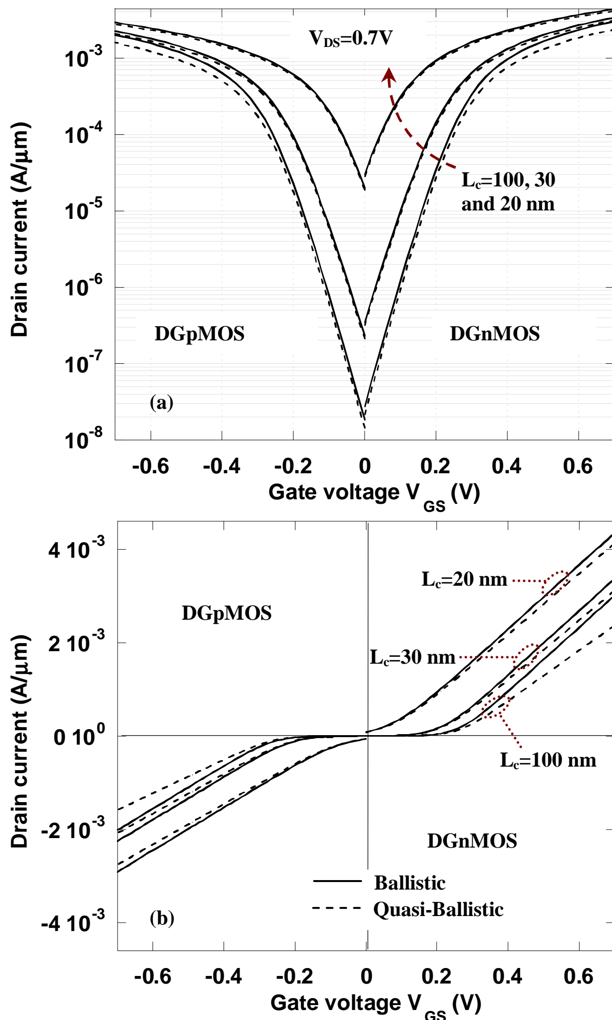

Figure 3: Drain current ((a) log and (b) lin scale) versus V_{GS} for L_c=100, 30 and 20 nm. Solid line for ballistic transport and dashed line for quasi-ballistic transport.

4 CIRCUIT SIMULATIONS

In addition to the simulation of single device operation, we have simulated different circuit elements such as CMOS inverters and ring oscillators (Fig. 1b and 1c) to show the impact of ballistic/quasi-ballistic transport at circuit level.

The output voltage (V_{out}) of the CMOS inverter switches more sharply from the “1” state to the “0” state in the ballistic case than in quasi-ballistic transport (Fig. 4). The commutation of the CMOS inverter depends on the limit between linear and saturation region, which controls the switch between transistors. When SCE/DIBL occur, the transition between linear and saturate regime is modified, and the switch from the “1” state to the “0” state is less sharp. In the quasi-ballistic case, the abruptness of the CMOS characteristic is strongly deteriorated. In conclusion, these results prove that the ballistic transport improves the commutation and the static performances of the CMOS inverter.

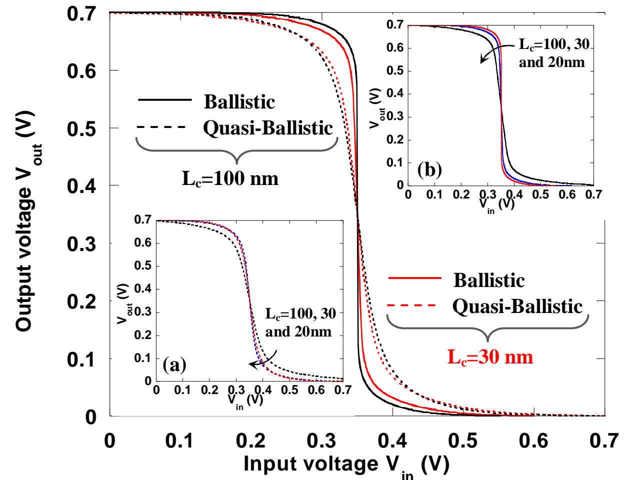

Figure 4: V_{out} versus V_{in} in a CMOS inverter. [Inset (a) and (b): transfer curve in ballistic and quasi-ballistic case for L_c=100, 30 and 20nm].

Figure 5 shows the oscillation frequency as a function of the charge capacitance for two channel lengths: 100 and 30 nm. As expected the oscillation frequency is reduced when the charge capacitance increases, due to variation of the propagation time through the inverters. We can also note the strong influence of short channel effects that increase the current value and reduce the difference between the oscillation frequencies in quasi-ballistic transport compared with ballistic transport.

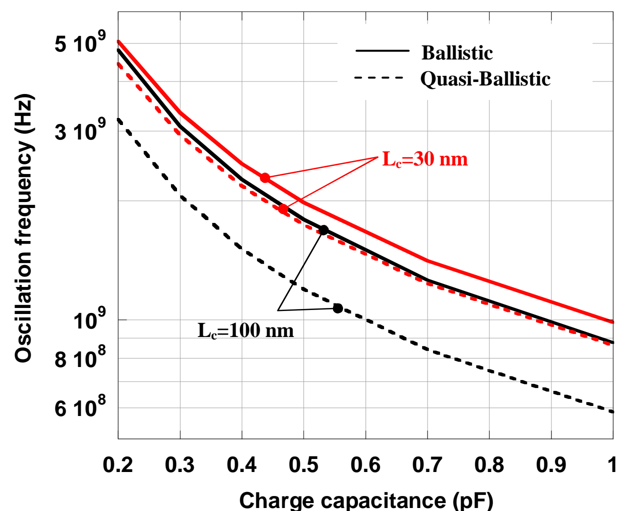

Figure 5: Oscillation frequency versus the charge capacitance for Lc=100 and 30nm

Moreover, we thoroughly studied the influence of parasitic elements and phenomena on circuit performances. Figure 6.a illustrates the impact of two charge capacitances on the oscillation frequency versus channel length. Figure 6.b shows the I_{on} current and V_T versus the channel length.

This last figure demonstrates the strong influence of SCE/DIBL effect on the transient performance. The explanation is that when SCE/DIBL effects occur:

- Firstly, the benefit of ballistic transport (versus quasi-ballistic) on the commutation of the CMOS inverters is hidden (inset (a) and (b) of figure 4).
- Secondly, the I_{on} current is strongly increased (figure 6.b).

Consequently the oscillation frequency in ballistic and quasi-ballistic case is less influenced by the value of the dynamic mean free path.

These results show that the oscillation frequency is directly influenced by the type of transport (ballistic versus quasi-ballistic) which changes strongly the static and the transient performances. But parasitic phenomena such as interconnect capacitances or SCE/DIBL are essential parameters in the analysis of circuit performances even when the intrinsic behaviour of transistors is dominated by ballistic transport.

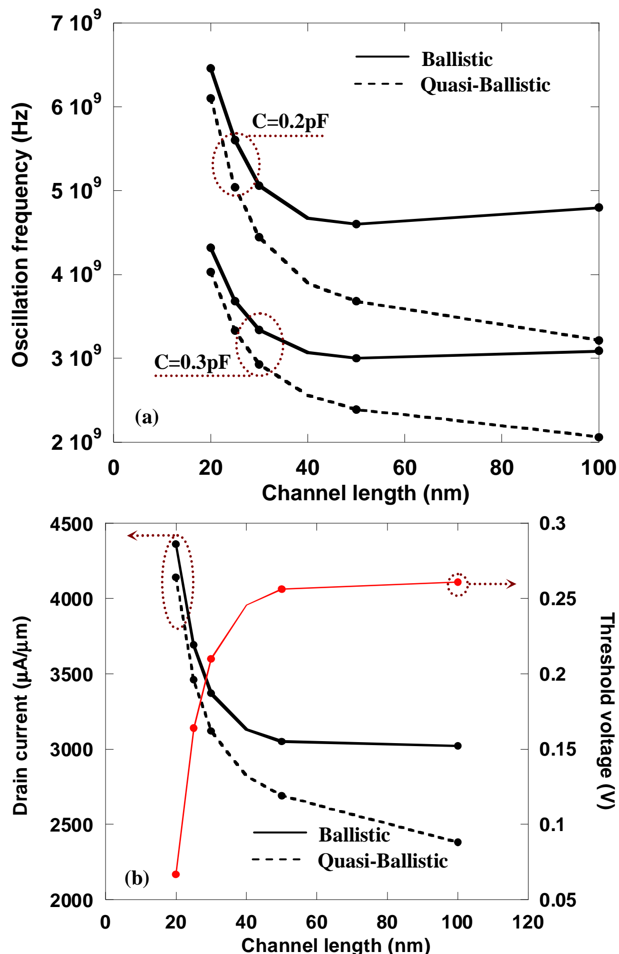

Figure 6: (a) Oscillation frequency versus the channel length for C=0.2 and 0.3 pF. (b) Drain current at V_{DS}=V_{GS}=0.7V and V_T versus the channel length.

5 CONCLUSION

In this work, a compact model for DGMOS taking into account ballistic and quasi-ballistic transport has been proposed and implemented in Verilog-A environment. Short channel effects and an interpolation function to link the above and the subthreshold voltage have been included to obtain a complete description of current characteristics. The dynamical mean free path definition was used to describe scattering processes with impurities and phonons. Finally, the model has been used to simulate two different small-circuits (CMOS inverter and ring oscillators) and to show the significant impact of ballistic/quasi-ballistic transport on the commutation of CMOS inverter and the oscillation frequency of ring oscillator. Our simulation results prove that the ballistic transport improves the commutation and the static performances of the CMOS inverter, and increases the oscillation frequency of ring oscillators.

This work also demonstrates the feasibility of a simulation study of ballistic/quasi-ballistic transport at circuit level and highlights the direct relation between the type of transport and static or transient performances of small-circuits.

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REFERENCES

[1] M. Lundstrom and Z. Ren, “Essential physics of carrier transport in nanoscale MOSFETs”, *IEEE Trans. Electron Devices*,vol. 49, no. 1, pp. 131-141, Jan. 2002.

[2] M. Lundstrom, “Elementary scattering theory of the Si MOSFET”, *IEEE Trans. Electron Device Lett.*, vol. 18, no 7,pp. 361-363, Jul. 1997.

[3] K. Natori, “Ballistic metal-oxide-semiconductor field effect transistor “, *J. Appl. Phys.*, vol. 76, no. 8, pp. 4879-4890, Oct. 1994.

[4] E. Fuch *et al*, “A new bascattering model giving a description of the quasi-ballistic transport in Nano-MOSFET”, *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2280-2289 Oct. 2005.

[5] K. Suzuki *et al*, “Analytical threshold voltage for short channel n+-p+ double-gate SOI MOSFETs”, *IEEE Trans. Electron Devices*,vol 43, no 5, pp732-738, May. 1996.

[6] F.Assad *et al*, “Performance limits of silicon MOSFET’s“, *IEEE IEDM Tech. Dig*, 1999.