Self-Consistent Thermal Electron-Phonon Simulator for SOI Devices

S. M. Goodnick*, K. Raleva** and D. Vasileska*

*Arizona State University, Tempe, AZ 85287-5706, USA
**FEIT-UKIM, Skopje, Republic of Macedonia

ABSTRACT

To investigate the role of self-heating effects on the electrical characteristics of nano-scale devices, we implemented a two-dimensional Monte Carlo device simulator that includes the self-consistent solution of the energy balance equations for both acoustic and optical phonons. The acoustic and optical phonon temperatures are fed back into the electron transport solver through temperature dependent scattering tables. The electro-thermal device simulator was used in the study of different generations of nano-scale fully-depleted (FD) Silicon On Insulator (SOI) devices that are either already in production or will be fabricated in the next 5-10 years. We find less degradation due to self-heating in very short channel device structures due to increasing role of non-stationary velocity overshoot effects which are less sensitive to the local temperature.

Keywords: heating effects, nanoscale devices, phonons, BTE, Monte Carlo method

1 INTRODUCTION

Heat conduction in dielectric materials and most semiconductors is dominated by lattice vibrational waves. The basic energy quantum of lattice vibration is called a phonon, analogous to a photon which is the basic energy quantum of an electromagnetic wave. Similar to photons, phonons can be treated as both waves and particles. Size effects appear if the structure characteristic length is comparable to or smaller than the phonon characteristic lengths. Two kinds of size effects can exist: the classical size effect, when phonons can be treated as particles, and the wave effect, when the wave phase information of phonons becomes important. Phonon-boundary scattering is responsible for a large reduction in the thermal conductivity of a thin silicon layer where the thickness of the film is comparable to or smaller than the phonon mean free path, Λ.

The lateral thermal conductivity of the thin silicon layer decreases as the thickness of the film is reduced. Deviation of the thermal conductivity from the bulk value takes a sharp dive as the thickness of the film is reduced beyond 300 nm, which is the order of magnitude for the phonon mean free path in silicon at room temperature. For example, the thermal conductivity of the 20 nm thick silicon layer is nearly an order of magnitude smaller than the bulk value.

It should also be mentioned that the Fourier heat conduction equation cannot explain the thickness dependency of thermal conductivity in silicon. The impact of phonon-boundary scattering on the thermal conductivity of a thin silicon layer can be predicted using the Boltzmann Transport Equation (BTE) for phonons.

On the other hand, it is well known that heat generation and the associated thermal management in very large scale integrated (VLSI) circuits (or nanoscale devices) is one of the major barriers to further increase clock speeds and decrease of feature size. The modern semiconductor industry benefits greatly from device scaling for the purpose of improving the device performance and reducing the manufacturing cost [1]. It is predicted that, when the device dimension scales down for a factor of F, the power consumption density usually increases by a factor of F^2 or F^3 for the case of constant voltage scaling. Also, for conventional complementary metal–oxide–semiconductor (CMOS) devices, by scaling them down to nanometer dimensions, it was predicted that the characteristic *phonon hot spot region* [2] near the drain would not scale proportionally. The size of the phonon hot spot is on the order of the magnitude of the high electric field region near the drain in a 180 nm device. What happens in nanoscale devices is very difficult to predict. As it will be seen from the presented simulation results, in nano-scale transistors, self-heating has a less detrimental effect when compared to larger structures due to the fact that velocity overshoot dominates carrier transport, and there is less exchange of energy between the electron system and the phonon bath [3, 4]. While this result does not mean that one does not have to be concerned with heating in nanoscale devices; it only means that we mainly have to focus on efficient ways of removing the heat from the device active region with, for example, state of the art Peltier coolers. Note that the predictions regarding heating in devices becomes more complicated with the fact that for channel lengths below 35 nm [5], various non-classical transistor structures will likely take over due to their delivery of higher performance with lower leakage current than traditional scaled CMOS approaches. New transistors, particularly ultra-thin-body (UTB) and double-gate MOSFETs, offer paths to further scaling, perhaps to the end of the 2006 International Technology Roadmap for Semiconductors (ITRS). In UTB-SOI, power consumption is drastically reduced along with leakage current and the devices show promise for high-performance CMOS, microprocessors and system-on-a-chip designs. In UTB-SOI structures [6], control of short-channel effects (SCE) and threshold voltage (V_t) adjustment can be realized with little or no channel doping. However, an issue that has shown to be important for the SOI devices is lattice heating. Heating effects arise

in SOI devices because the device is thermally isolated from the substrate by the buried oxide layer. No simulator can properly predict the electrical characteristics of nano-scale devices if it does not treat electron transport correctly; in particular non-stationary velocity overshoot effect. In particular, simulators that rely on energy balance models for the electronic transport typically overestimate or underestimate velocity overshoot due to the improper choice of the energy relaxation times taken from bulk calculations.

In the present work, we solve the Boltzmann transport equation for electrons using the Ensemble Monte Carlo (EMC) method coupled moment expansion equations for the phonons, both acoustic and optical. The coupling of electrons and non-equilibrium phonons has been studied for many years, and was included, e.g. in EMC simulations to study photoexcited carrier relaxation in quantum wells [7,8], and more recently by Alam and Lundstrom [9] to simulate laser diodes. However, these models are essentially momentum space models, and do not address spatially varying systems such as short channel transistors. Recently, there have been studies on describing thermal effects in devices that couple the Monte Carlo/Poisson approach to electro-thermal modeling [10,11] in SOI and Nitride devices. In that work, a somewhat simplistic model for non-equilibrium phonons is taken which does not distinguish the acoustic and the optical phonons as separate subsystems.

Because SOI devices consist of two distinct regions, the silicon device layer and the buried oxide layer (in which the phonons have significantly smaller mean-free paths), the phonon BTE is solved in the silicon layer to accurately model heat transport, but the simpler heat diffusion equation is used in the amorphous BOX because the characteristic length-scale of conduction is much smaller than the film thickness. The two distinct computational regions are coupled through interface conditions that accounts for differences in material properties. For the coupling of the silicon and oxide solution domains, it is necessary to calculate the flux of energy through the interface between the two materials at each point along the interface for every time step.

The boundary conditions used have been chosen based on those typically used in commercial simulators. The Silvaco ATLAS simulation package [12] (THERMAL3D module) states that the only thermal contact should be the substrate. We have performed simulations on our structure to verify this assertion with and without the silicon substrate present, and concluded that due to the large thermal conductivity of bulk Si, a 300K boundary condition on the bottom contact maps well into 300K boundary condition on the bottom of the BOX. In other words, the presence of the bottom silicon substrate does not affect either the electrical or the thermal characteristics of the structure being considered. Also, according to prescriptions given in the Silvaco ATLAS package, the source and drain should be left floating and the only electrode where one should specify isothermal boundary conditions is the gate. In fact, in the paper itself we change the thickness of the gate metal and the boundary condition at the end of the gate has not much influence on the current degradation. In these simulations, except at the boundary, we treat the metal gate as a material characterized with its own thermal conductivity. Since current nano-scale devices use metal gates to avoid poly-silicon depletion, such an assumption isothermal also is seemingly justified. However, to study the efficacy of the gate as a heat sink, we simulate the effect on the current of several different temperatures for the gate.

2 INFLUENCE OF THE BOUNDARY CONDITION ON THE GATE ELECTRODE ON THE ON-CURRENT

To properly solve the phonon balance equations, the device should be attached to a heat sink somewhere along the boundary or finite heat conduction through the surface should be allowed for. In our code, a heat sink is modeled by a simple Dirichlet boundary condition (i.e. constant temperature). We use the gate electrode contact and the bottom of the BOX as heat sinks. Table 1 gives the percentage of the current decrease due to the heating effects with the variation of gate electrode temperature. The calculated results show that the current degradation is more prominent for higher gate temperatures. When the temperature of the bottom of the BOX was set to the same values as given in Table 1, the current degradation was around 1%, so in all other simulations the temperature of the bottom of the BOX was set to 300K.

Table 1 Current variation with gate temperature for 25 nm fully-depleted SOI device structure with SiO2 as gate oxide.

Type of simulation	*Gate Temperature*	***Current Decrease***
thermal	300K	5.1%
thermal	400K	9.18%
thermal	600K	17.12%

Figure 1 show the velocity profile along the channel for the same bias conditions (Vgs=Vds=1.1 V) and different gate temperatures, where, as can be seen, the velocity in the channel decreases with the increase of the gate temperature, but the carriers in the channel are still in the velocity overshoot regime. As seen from the temperature maps of acoustic phonons in Figure 2, the lattice temperature in the source, the channel and the drain region is increasing with the increase of the gate electrode temperature, which means that the increased lattice temperature has larger impact on the decrease of the carrier velocity in the channel.

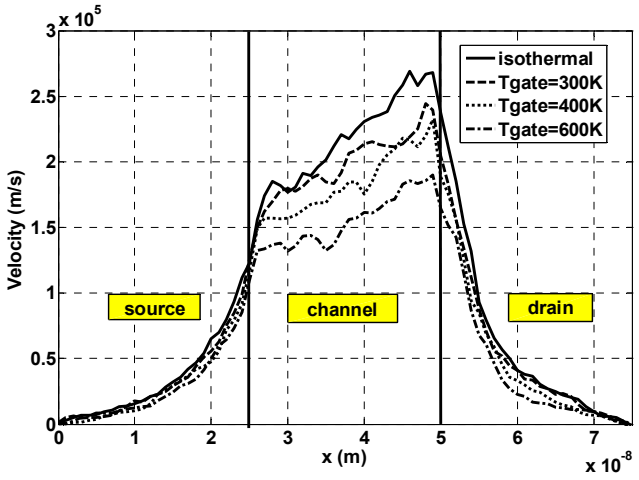

Fig. 1 Velocity along the channel for Vgs=1.1 V and Vds=1.1 V for different gate temperatures. Notice that the electrons are in the velocity overshoot regime.

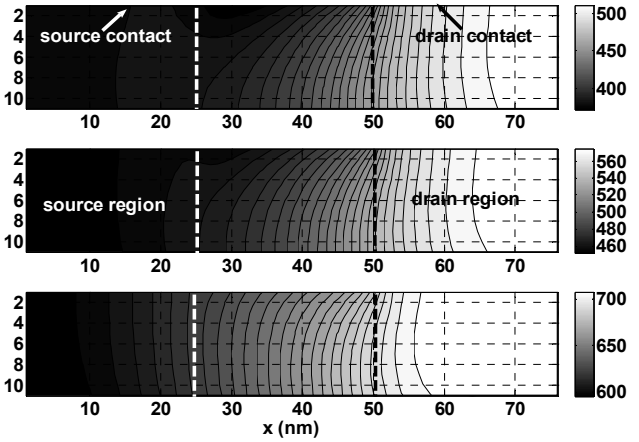

Fig. 2 Lattice temperature profiles in the silicon layer in 25 nm gate-length fully-depleted SOI MOSFET for Vgs=1.1 V and Vds=1.1 V and different gate electrode temperatures (300K, 400K and 600K from up to down). SiO2 is used as gate oxide.

3 THERMAL DEGRADATION WITH SCALING OF DEVICE GEOMETRY

In addition to the previously noted observation regarding the influence of the velocity overshoot, we modeled larger fully-depleted SOI device structures and we also investigated the influence of the temperature boundary condition on the gate electrode on the current degradation due to heating effects. The calculated results show that the current degradation is more prominent for larger devices and for higher gate temperatures. For 80 nm and larger devices, simulated carriers are not in the velocity overshoot regime in the larger portion of the channel (especially near the source end of the channel). Snapshots of the lattice temperature profiles in the silicon layer for these devices when the gate temperature is set to 300K, are given in Figure 3 and 4. From these snapshots one can observe that: a) the temperature in the channel is increasing with the increase of the channel length, b) the maximum lattice temperature region (hot spot) is in the drain and it shifts towards the channel for larger devices. This behavior is more drastic for higher gate temperatures.

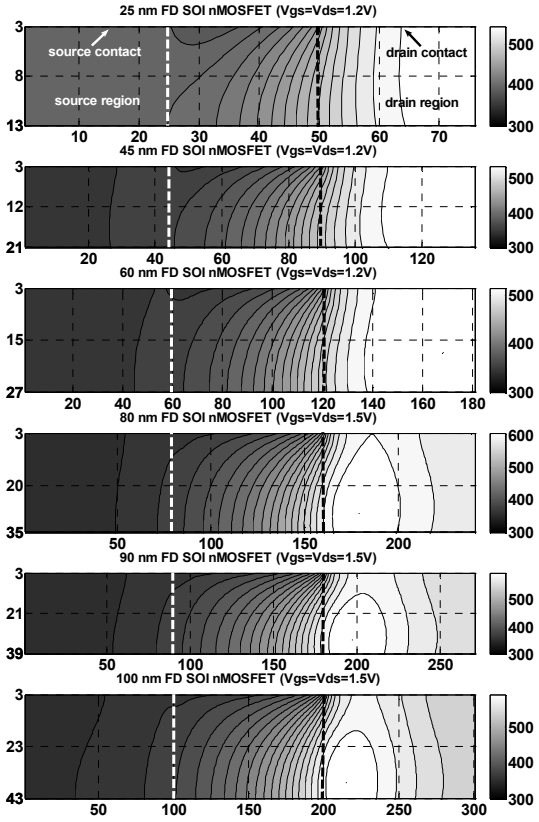

Fig. 3 Lattice temperature profiles in the silicon layer for FD SOI MOSFETs with gate temperature set to 300K. (25 nm –top, 100 nm-bottom).

4 CONCLUSIONS

A self-consistently coupled thermal/Ensemble Monte Carlo device simulator has been developed and applied to the study of fully-depleted SOI devices. We show that the pronounced velocity overshoot present in the nanometer scale device structure considered in the present study minimizes the degradation of the device characteristics due to lattice heating. This observation was also justified with SILVACO Atlas simulations that demonstrated that for larger energy relaxation times, that correspond to the case of more pronounced velocity overshoot, current degradation in the on-state due to thermal effects is on the order of 10%, not to 30% as found in larger device structures in which velocity overshoot does not play significant role.

We also investigate the influence of the gate temperature on the amount of current degradation due to heating effects. Namely, we used the gate contact as a heat sink to

solve properly the phonon balance equations. As seen from the temperature maps of acoustic phonons presented in the paper, the lattice temperature in the source, channel and drain region is increasing with the increase of the gate temperature, which means that the increased lattice temperature has larger impact on the decrease of the carrier velocity in the channel. When examining heating in different device technologies, we observed a bottleneck between the lattice and the optical phonon temperature in the channel which is more pronounced for shorter devices, due to the fact that the energy transfer between optical and acoustic phonons is relatively slow compared to the electron-optical phonon processes and the fact that the electrons are in the velocity overshoot (and since the channel is very short, they spent little time in the channel).

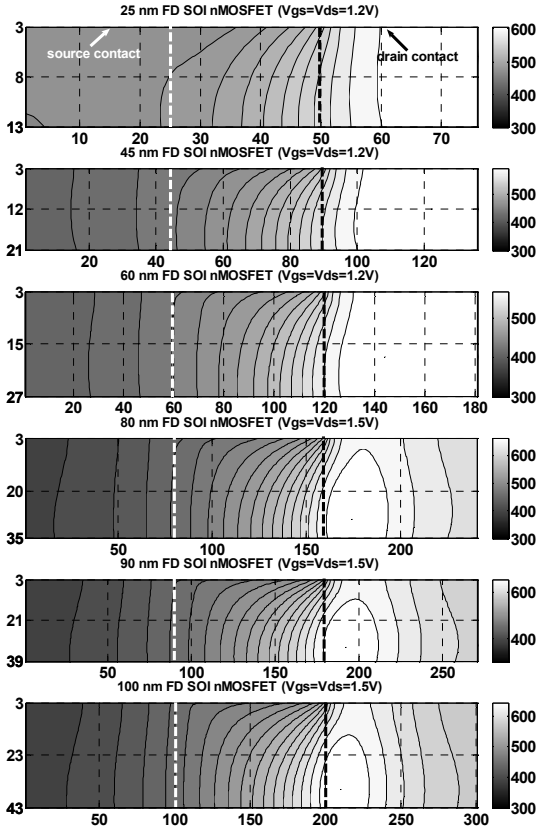

Fig. 4 Optical phonon temperature profiles in the silicon layer for FD SOI MOSFETs with gate temperature set to 300K. (25 nm –top, 100 nm-bottom).

To better understand the phonon temperature bottleneck, different cross-sections of the lattice and the optical phonon temperature profiles in the channel direction were investigated. Briefly, we find that the bottleneck is decreasing from Si/SiO_2 interface to Si/BOX interface. For shorter devices, it exists in the whole channel region, which is not a case for longer devices (thicker Si-layer and longer channel length). From the results we have presented here and those we have published earlier one can conclude that the higher the temperature in the channel and/or the longer the electrons are in the channel, the larger the degradation of the device electrical characteristics is due to the heating effects.

REFERENCES

[1] R. Chau, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros, M. Metz, "Silicon nano-transistors and breaking the 10 nm physical gate length barrier", *Device Research Conference*, pp. 123-126 (2003).

[2] E. Pop, K. Banerjee, P. Sverdrup, R. Dutton and K. Goodson, "Localized Heating Effects and Scaling of Sub-0.18 Micron CMOS Devices", *IEDM Techn. Dig*., 679 (2001).

[3] K. Raleva, D. Vasileska and S.M. Goodnick, accepted for publication in *Journal of Computational Electronics*, 2008.

[4] Katerina Raleva, Dragica Vasileska, and Stephen M. Goodnick, "The Role of the Temperature Boundary Conditions on the Gate Electrode on the Heat Distribution in 25 nm FD-SOI MOSFETs with SiO2 and Gate-stack (High-K Dielectric) as the Gate Oxide", *accepted for presentation at the ISDRS, Washington DC December 12-14,* 2007.

[5] IA Technology Roadmap for Semiconductors, 2003 (http://public.itrs.net/).

[6] T. Numata and S.-I. Takagi, "Device design for sub-threshold slope and threshold voltage control in sub-100 nm fully-depleted SOI MOSFETs", *IEEE Trans. Electron Devices*, Vol. 51, pp. 2161-2167 (2004).

[7] P. Lugli and S.M. Goodnick, "Non-Equilibrium LO Phonon Effects in GaAs/AlGaAs Quantum Wells", *Phys. Rev. Lett.* Vol. 59, pp. 716-719 (1987).

[8] S. M. Goodnick and P. Lugli, "Hot Carrier Relaxation in Quasi-2D Systems," in Hot Carriers in Semiconductor Microstructures: Physics and Applications, (J. Shah, Ed.), Academic Press Inc., pp. 191-234, 1992.

[9] M. A. Alam and M. S. Lundstrom, "Effects of Carrier Heating on Laser Dynamics – A Monte Carlo Study", IEEE J. Quantum El. Vol. 33, pp.2209-2220 (1997).

[10] T.Sadi, R.W.Kelsall and N.J.Pilgrim, "Electrothermal Monte Carlo Simulation of Submicrometer Si/SiGe MODFETs", IEEE Trans. on Electron Devices, Vol.54, No.2, February 2007.

[11] T. Sadi, R.W.Kelsall and N.J.Pilgrim, "Electrothermal Monte Carlo simulation of submicron wurtzite GaN/AlGaN HEMTs", J.Comput.Electron. (2007) 6:35-39.

[12] Silvaco Inc.