Tunnel Field Effect Transistor (TFET) with Strained Silicon Thinfilm Body for Enhanced Drain Current and Pragmatic Threshold Voltage

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ABSTRACT

Quantum tunneling devices are very promising as they have very low leakage current and show good scalability. However, the most serious drawback for tunneling devices hampering their wide-scale CMOS application is their low on-current and high threshold voltage. In this paper, we propose a novel lateral Strained Double-Gate Tunnel Field Effect Transistor (SDGTFET), which not only tackles these problems very well but also shows excellent overall device characteristics. For the first time, using two dimensional simulation, we show that the proposed device improves the on-current by two-order of magnitude without significantly degrading the off-current, lowers the threshold voltage so as to meet the ITRS guideline, improves the average subthreshold swing and also shows good immunity to short channel effects.

Keywords: **Tunneling, Strained-Silicon, SOI MOSFET, Short-channel Effects, TFET, Two-dimensional simulation.**

1 INTRODUCTION

With the reducing device dimensions, the problem of leakage current becomes more prominent. Novel devices utilizing quantum tunneling phenomenon as the operating principle show good promise. These devices have very low leakage current, have excellent subthreshold swing and exhibit good scalability [1]-[4]. However, the most serious drawback for tunneling devices is their low on-current and high threshold voltage [2]-[4]. This problem needs to be tackled so that these devices could be employed for wide-scale CMOS application. In this paper, we propose a novel lateral Strained Double-Gate Tunnel Field Effect Transistor (SDGTFET), which not only tackles these problems very well but also shows excellent overall device characteristics.

2 DEVICE STRUCTURE AND SIMULATION MODEL

A schematic cross-sectional view of the proposed SDGTFET device is shown in Fig.1. The structure of this device is similar to the conventional Double Gate Tunnel Field Effect Transistor (DGTFET) [3]. However, the silicon body of this device is strained silicon. This device can be fabricated using single-layer strained-silicon-on-insulator (SSOI) technology [5], [6]. The amount of strain in an SSOI is controlled by varying the mole fraction of Ge in the relaxed SiGe buffer layer that is used during its fabrication. The device parameters used in our simulations are as follows: Source doping = $10^{20}/cm^3$, Drain doping = $5x10^{18}/cm^3$, Channel doping = $10^{17}/cm^3$, Gate length = 50 nm, Gate oxide thickness = 3 nm, Silicon body thickness = 10 nm, Gate work function = 4.5 eV, Drain bias, V_{DS} = 1 V. Ge mole fraction in the SiGe buffer layer, x is varied from 0 to 0.5. Using two-dimensional simulation, we show how the modulation of band-structure of silicon (engineered by straining) results in an overall improvement of the device characteristics of an SDGTFET. The simulation model use drift-diffusion model for current transfer. Non-local band-to-band tunneling is turned on in our simulations. A very fine mesh is defined in the simulation structure and especially in the regions where tunneling takes place.

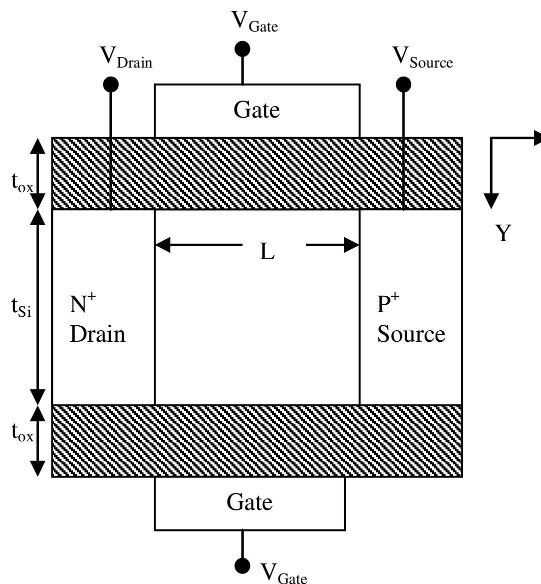

Figure 1 Cross-sectional view of an SGTFET

3 SIMULATION RESULTS

An extensive simulation of this device structure was done so as to study the performance of the device. The transfer characteristics of the SDGTFET at different Ge mole

fractions were computed using simulations. The on-current of the device, defined as the drain current at a particular gate voltage, was extracted from these transfer characteristics.

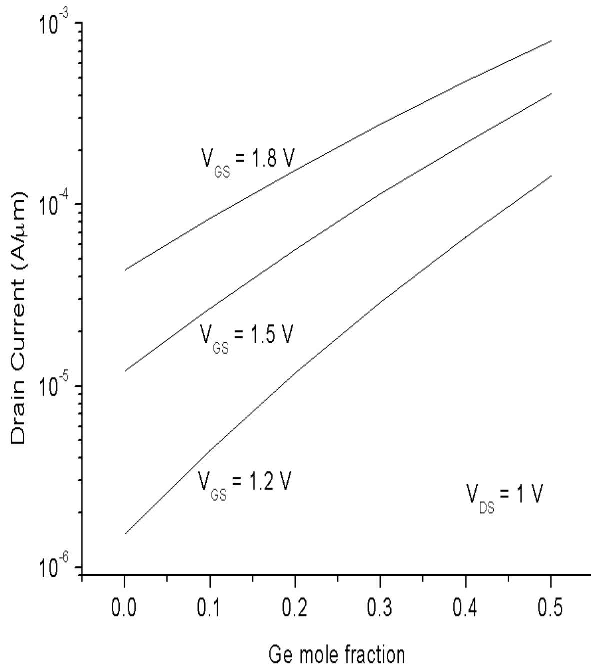

Figure 2 Drain Current of an SDGTFET versus Ge mole fractions at different V_{GS}

It can be easily seen from Fig. 2 that the on-current of the device improves by two-order of magnitude for a Ge mole fraction of 0.5. The on-current of the unstrained device (Ge mole fraction = 0) is in range of tens of µA/µm which fails miserably to meet the ITRS near-term low power guideline of around 700 µA/µm. However, as the Ge mole fraction is increased, the on-current comes closer to meeting this guideline. In fact, at Ge mole fraction of 0.5, this device is capable of meeting the ITRS guideline. It should be mentioned that though the on-current improves for an SDGTFET, the off-current does not degrade significantly. The ratio of on-current to off-current was extracted from the transfer characteristics. It was found that this ratio improves initially with increasing Ge mole fraction. But at mole fraction greater than 0.2, this ratio starts degrading a little with increasing Ge mole fraction (due to increase in off current). In fact the ratio of on-current to off-current was found to attain a maximum value at a Ge mole-fraction of around 0.2. Also, since the complete device is strained, the improvement in device characteristics can be derived in both NMOS and PMOS type of operations.

The threshold voltage of an SDGTFET was extracted from the simulation results. For an unstrained SDGTFET (Ge mole fraction 0), the threshold voltage is around 0.9 V which is much higher than the ITRS near term low-power threshold voltage requirement of around 0.3 V. As the Ge mole fraction is increased the threshold voltage of this device decreases. For a mole fraction of 0.5, the threshold voltage can be decreased to around 0.4 V, which is much closer to the abovementioned ITRS guidelines.

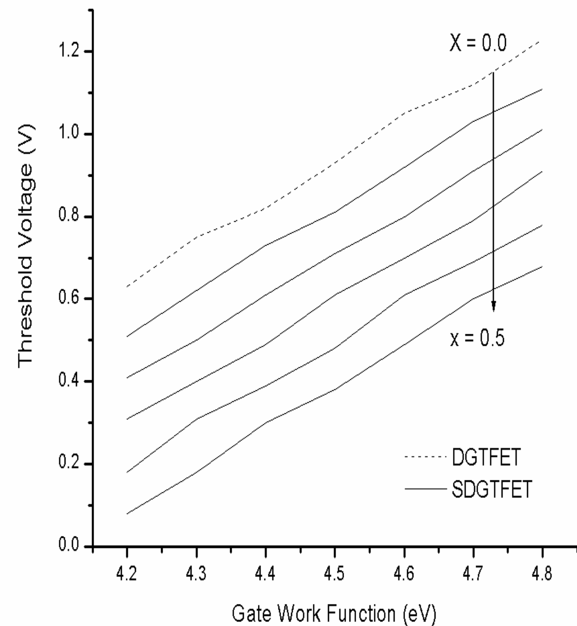

Figure 3 Threshold voltage versus gate workfunction of DGTFET and SDGTFET for different Ge mole fractions

Further reduction in threshold voltage can be brought about by gate work-function engineering. Fig. 3 shows the variation of threshold voltage with the change in gate work-function. However, it should be noted that the reduction in threshold voltage with reduction in gate work-function is accompanied by an increase in off-state leakage. Fig. 4 shows the transfer characteristics of the device at different work function for a Ge mole fraction of 0.2. It can easily be inferred from this figure that there is an increase in off-state leakage at lower work function. Hence a tradeoff needs to be made to get the desired threshold voltage without sacrificing the on-current by off-current ratio.

The subthreshold swing of an SDGTFET was extracted from our simulation results. Since, the subthreshold behavior of tunneling devices is a strong function of gate voltage, classical definition of subthreshold swing cannot be used for these devices. The point subthreshold slope and the average subthreshold slope as defined in [3] were used in our simulation study. It was found that an SDGTFET shows considerable improvement in both point subthreshold slope and average subthreshold slope. In fact, an SDGTFET shows average subthreshold slope better than 60 mV/decade (that of an ideal MOSFET) for a Ge mole fraction of 0.4 or more.

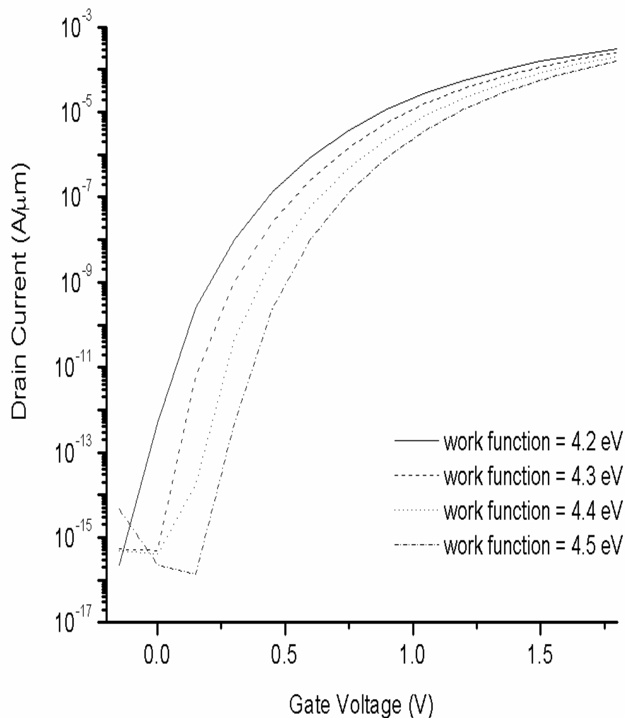

Figure 4 Transfer characteristics of an SDGTFET with x = 0.2 for different gate workfunction

The short channel effects in an SDGTFET were also studied. It was found that an SDGTEFT show negligible threshold voltage roll-off up to 20 nm channel length. The transfer characteristics of an SDGTEFT do not change appreciably with the change in channel length. The primary reason for this is that the tunneling phenomenon is confined to a very narrow region around the source in an SDGTFET. Hence, decreasing the gate length does not have much effect on the transfer characteristics until the drain is too close to the source to impact the tunneling phenomenon. Therefore, it can be concluded that an SDGTEFT is very much immune to short channel effects.

4 CONCLUSIONS

For the first time, using two-dimensional simulation, we have shown that the proposed SDGTFET is a very good candidate for low-leakage CMOS technology. Also, since the device structure is similar to the strained DGFET technology, this can be seamlessly integrated into the existing process flow. Using two-dimensional device simulation we have shown that this device meets the ITRS guidelines in terms of on-current and threshold voltage, has excellent subthreshold slope and negligible short channel effects. Hence this device looks promising to take the center stage of CMOS technology in the times to come.

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