Neural Computational Approach for FinFET Modeling and Nano-Circuit Simulation

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ABSTRACT

The present paper demonstrates the suitability of artificial neural network (ANN) for non-linear modeling of a FinFET for RF applications. FinFET used in this work is designed using careful engineering of source drain extension (SDE) regions, which simultaneously improves transit frequency (f_T) and dc gain $A_{V0} = (g_m / g_{ds})$. The framework for the ANN based FinFET model is a common source large-signal equivalent circuit, where the dependence of intrinsic capacitances, resistances and dc drain current (I_d) on drain-source (V_{ds}) and gate-source (V_{gs}) bias is derived by two-layered neural network architecture. All extrinsic components of the FinFET model are treated as bias independent. The model is implemented in a circuit simulator and verified by the model ability to generate acceptable I_d and circuit parameters to the excitations not used during training. FinFET based on low noise amplifier (LNA) at ~15μA/μm gives ~18.5dB improvement in A_{V0} and nearly identical third-order-intercept (IIP_3) when compared to an identical size bulk MOSFET.

Keywords: Artificial Neural Network, FinFET, Non-linear Modeling, Nano-Circuit, Low Noise amplifier.

1 INTRODUCTION

FinFETs are very promising for low power, low voltage portable applications [1]. For nano-circuit simulation, a suitable FinFET model is required. As the MOSFET dimensions are scaled below 50 nm, it is very difficult to develop physics based compact models [2]. In recent years artificial neural network (ANN) has been used for modeling of variety of transistors [3] [4], as it avoids repeated solving of the complex transcendental equations of a traditional compact physical model, but still offers sufficient accuracy. An ANN model is either based on direct [5] or indirect equivalent circuit approach [3][4]. In the equivalent circuit shown in Fig. 1, both non-linear dc and dynamic (ac) behavior can be modeled simultaneously. While a similar indirect approach has been used for other devices [3] [4], this is the first application for FinFET modeling. 3D ATLAS [6] has been used to simulate a FinFET, which comprises of gate length (L_g) = 60 nm, fin height (H_{fin}) = 60 nm, fin width (T_{fin}) = 42 nm and T_{OX} = 2.2 nm as shown in Fig. 2. Details of measured results have been outlined [7]. This FinFET has since been redesigned for optimal low power performance, with careful engineering of gate–source/drain underlap region, to simultaneously maximize both f_T and dc gain A_{V0} [8]. Source/drain profile was modeled using the expression $N_{SD}(x) = (N_{SD}(x))_{peak}\, exp(-x^2/\sigma^2)$, where $(N_{SD}(x))_{peak}$ is the peak source/drain doping, σ (lateral straggle) defines the roll-off [9] of source/drain profile as $\sigma = \sqrt{2sd/ln(10)}$, where s is the spacer width and d the source/drain doping gradient [9] [10] evaluated at the gate edge $d = \left(\frac{1}{\left| dN_{SD}(x)/dx \right|} \right)$

Modeling of nanoscale SDE engineered devices for circuit applications involves formulation of short-channel effects (SCEs), velocity saturation, gate voltage dependent effective gate length (L_{eff}), source/drain (S/D) series resistance and voltage dependent mobility effects [2]. These physical effects are difficult to formulate specially for nano-scale devices. Therefore, in this work artificial neural networks (ANNs) are applied for FinFET modeling

The developed ANN model is implemented in circuit simulator. At both device and circuit level ANN model accuracy has been successfully demonstrated. At device level f_T of FinFET is comparable to the bulk MOSFET, whereas maximum frequency of oscillation (f_{max}) is nearly two times higher due to lower drain-to-source conductance (g_{ds}) and lower capacitance compared to bulk MOSFETs. However, FinFET LNA give better circuit performance in terms of A_{V0} and comparable linearity compared to bulk. Bulk MOSFET model is based on BSIM4 [11] model parameters, which is derived form nano-predictive technology model (PTM) [12] and used in this work for comparison.

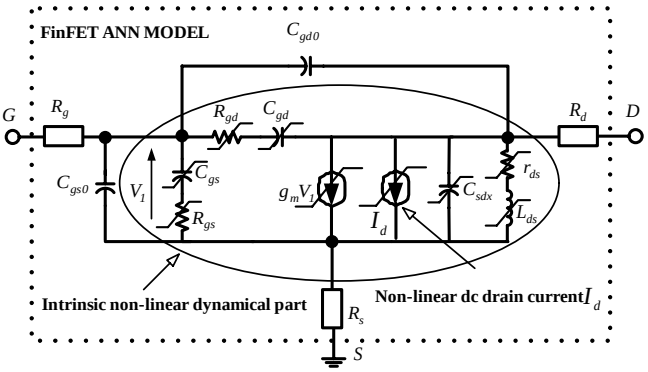

Fig. 1 Non-linear model for FinFET

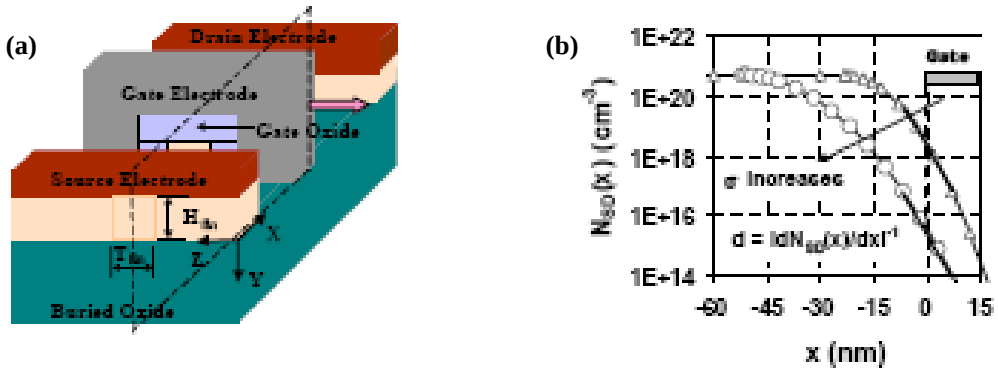

Fig. 2. **(a)** Schematic diagram of a FinFET analyzed in the present work, and **(b)** Variation of source doping profile for various σ values along the cut-plane along the channel as indicated by dashed lines.

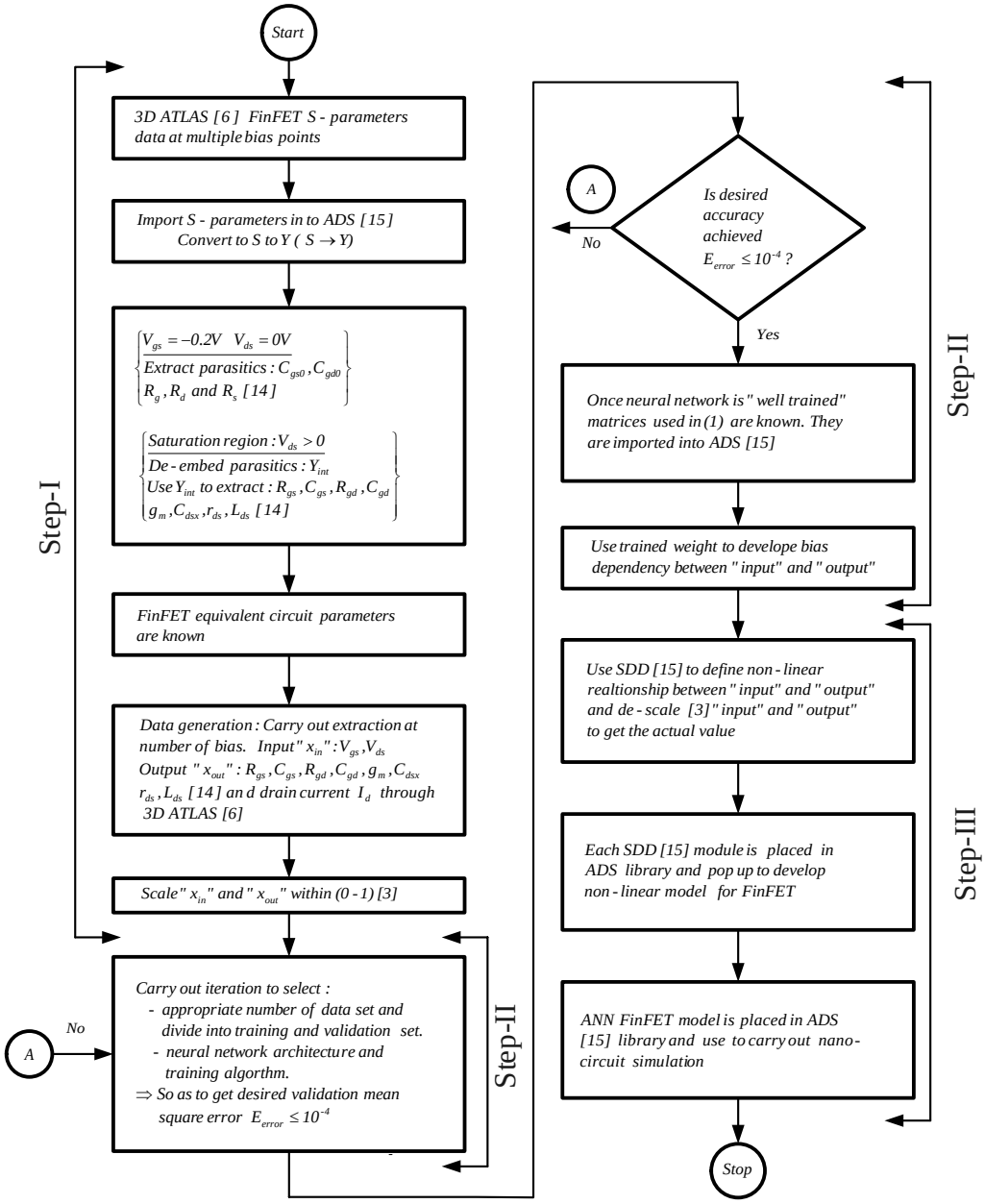

Fig. 3. Basic steps involved in FinFET model development and nano-circuit simulation

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2 NEURAL COMPUTATIONAL APPROACH

ANNs are mathematical tools used to represent the non-linear relationship between set of input data and a set of output data. In general, due to its architecture and choice of activation functions, an ANN model suffers less from convergence problems than the alternative polynomial functions [13]. Non-linear relation between bias voltages input x (V_{gs} and V_{ds}) and circuit parameters and I_d outputs y (R_{gs}, R_{gd}, C_{gd}, g_m, C_{dsx}, g_{ds}, L_{ds} and I_d) shown in Fig.1 is modeled using 2-layer ANN [3][4]. A total of 200 "normalized" samples of x and y (drain current I_d), scaled to lie within range 0 to 1, are split into training (125 samples) and testing (= validation) (75 samples) categories. Training and validation steps were run to find the optimal weight values for each parameter to minimize mean square error ($E_{rror} \le 10^{-4}$) between ANN prediction and original data in the bias range: V_g : -0.2 to 0.4 V and V_d : 0 V to 1.2V generated through 3D ATLAS. Using the same procedure as was done for drain current I_d, circuit parameters bias dependency were derived using 2 layered architecture. Test data samples for circuit parameters were created by carrying out $y-$parameter extraction [14] generated from 3D ATLAS simulation of a 60 nm FinFET with appropriate source-drain engineering [8]. Trained weights were imported into Advanced Design System (ADS) [15] where its Symbolically Defined Devices (SDD) feature was used to develop the non-linear relationship between x and y. The SDD modules for each circuit parameter were saved in ADS [15] library, and appropriately accessed from the top level to develop the non-linear model. The basic steps involved in ANN based model development is given in flow chart given in Fig. 3.

3 RESULTS AND DISCUSSION

To validate model, we first compared 3D ATLAS and modeled I_d for p- and n-channels FinFET. Fig. 4 compares predicted results (from ANN model) and 3D ATLAS [6] for current voltage characteristics $I_d - V_{gs}$ and $I_d - V_{ds}$. As can be seen from Fig. 4 that very good agreement between them is obtained over full bias range.

Table 1 gives an example of the excellent match between extracted [14] and ANN predicted circuit parameters. Fig. 5 compares FinFET f_T and f_{max} versus drain current density J_{ds} (μA/μm). Extrinsic resistances for source/drain and gate of 20Ω and 5Ω [7], [16], external to the ANN model based on detailed simulation and measurement, represent the best estimate of parasitic resistance for a 300 finger device. A similar design based on the "Predictive Technology Model"(PTM) for bulk MOSFET [12] with same parasitics gives higher f_T and f_{max} in FinFET technology. For an optimal FinFET design, a predicted two-fold enhancement in f_{max} over traditional bulk technology is due to lower g_{ds} and lower C_{gd}. Discrete measurement points in Fig. 5 represent reported values of f_T and f_{max} for a non-underlap SDE FinFET design [7]. Further improvement in f_{max} has been achieved from a more optimal underlap FinFET design [8].

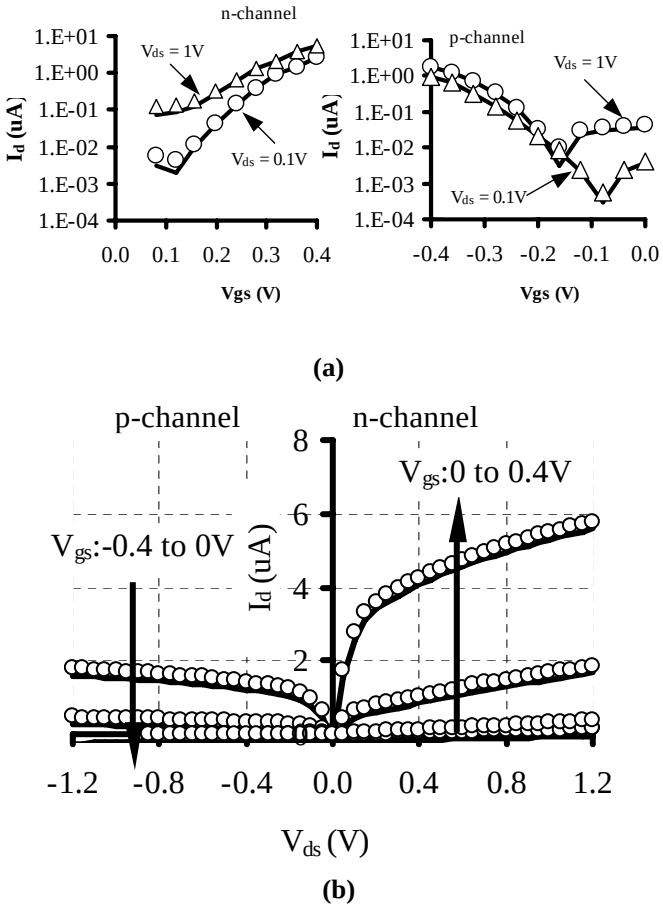

Fig. 4 DC current-voltage characteristics **(a)** $I_d - V_{gs}$ **(b)**. $I_d - V_{ds}$; Solid lines are results from ANN model and symbol from 3D ATLAS.

The ANN model has been utilized to design a 5GHz low noise amplifier (LNA) [18] matched to 50Ω source and load [19]. A FinFET design offers improvement at ~15μA/μm in both third-order-intercept IIP_3 (~1.5 dB) and A_{V0} (~18.5dB), compared to a bulk technology as illustrated in Fig. 6. This is due to higher $P_{IP3} = \frac{4}{50}\left(\frac{dI_d/dV_{gs}}{dI_d^3/dV_{gs}^3}\right)$ (i.e. better g_m linearity) [19] and lower g_{ds} in FinFET compared to bulk as given in Table 2. However, A_{V0} enhancement in FinFET degrades at high drain current due to high series resistance.

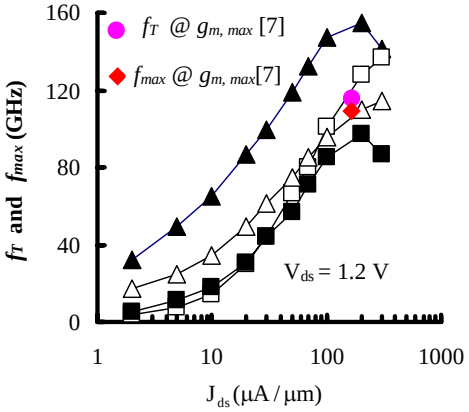

Fig. 5. Comparison of measured and simulated f_T and f_{max} from ANN for 300 fingers. Filled Symbol = FinFET; Open Symbol = Bulk; Line = 3D ATLAS

Table 1 : Extracted circuit -parameters for single finger FinFET

Overlap capacitances (V_{gs} = -0.2 V V_{ds} = 0.0 V)		
$C_{gd0} = C_{gs0}$	0.015 fF	
Circuit parameters (V_{gs} = 0.2 V V_{ds} = 0.2V)		
Parameters	Extracted [14]	ANN Model
R_{gd} (kΩ)	6.37	6.34
R_{gs} (kΩ)	5.47	5.43
100×C_{gd} (fF)	1.06	1.02
100×C_{gs} (fF)	2.27	2.25
100×g_{ds} (mS)	0.0134	0.013
100×g_m (mS)	0.178	0.176
L_{ds} (nH)	4339	4330
100×C_{dsx} (fF)	0.834	0.830

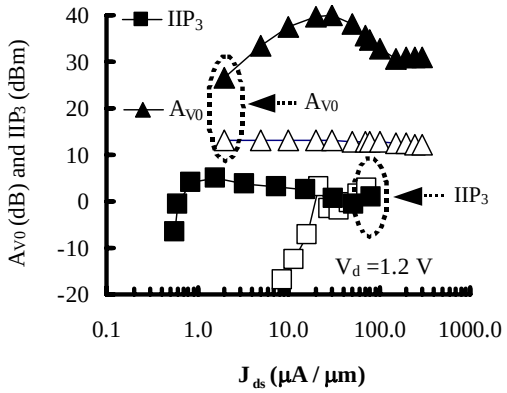

Fig. 4. Comparison of A_{V0} and IIP_3 for FinFET and bulk for 300 fingers. Filled Symbol = FinFET; Open Symbol =Bulk MOSFET

Table 2: Comparison of FinFET and bulk circuit parameters for 300 fingers (I_d =15μA/μm and V_{ds} = 1.2V)

Parameters	FinFET	Bulk
$g_{m1} = dI_{ds} / dV_{gs}$(A/V)	0.01928	0.0071
$g_{m3} = d^3I_{ds}/d^3V_{gs}$(A/V^3)	0.586	0.235
$P_{IP3} = (g_{m1} / g_{m3})\times$ (4/50)	2.63×10^{-3}	2.41×10^{-3}
$g_{ds} = dI_{ds} / dV_{ds}$ (A/V)	0.00265	0.0465

4 CONCLUSIONS

A behavioural model based on a neural network has been incorporated in a circuit simulator for simulation of FinFET based nano-circuits. The ANN model has been trained to predict y -parameters, which agrees closed with those extracted from precise 3D device simulations. A high frequency demonstrator LNA circuit based on the ANN model has been designed and simulated. Improved A_{V0} has been observed when design is based on FinFET, as opposed to bulk MOSFET. Performance enhancement can be directly attributed to lower g_{ds} and lower capacitance in FinFET.

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