Assessment of L-DUMGAC MOSFET for High Performance RF Applications with Intrinsic Delay and Stability as Design Tools

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ABSTRACT

The paper assesses RF performance of Laterally amalgamated DUal Material GAte Concave MOSFET (L-DUMGAC) MOSFET using ATLAS device simulator. The L-DUMGAC MOSFET design integrates the advantages of dual material gate architecture with the concave MOSFET. In this work, TCAD assessment is done by performing AC simulations at very high frequencies, and evaluating the RF figure of merits in terms of maximum available power gain (Gma), stern stability factor (K) and intrinsic delay. Results reveal that L-DUMGAC architecture exhibits a significant improvement in Gma & K; and an appreciable reduction in intrinsic delay, in comparison to its conventional counterpart: SIngle Material Gate Concave (SIMGAC) MOSFET; hence, strengthening the idea of using L-DUMGAC for switching applications, thereby giving a new opening for high frequency wireless communications.

Keywords: ATLAS, L-DUMGAC, intrinsic delay, stability, and RF.

1 INTRODUCTION

Silicon device technology has become an attractive low cost solution for many high frequency personal communication products. With scaling of the device dimensions into the sub-50-nm regime, the transistors have achieved cutoff frequencies in the range of several GHz, making CMOS technology suitable for wireless communications and other RF applications [1-2]. However, undesirable short-channel effects, the mobility degradation and increased parasitic capacitances drastically reduce the device transconductance, voltage gains and noise performance making the scaled technologies unsuitable for analog/RF applications [3].

Concave MOSFETs [4-5] are known to alleviate the short channel effects and the hot carrier effects appreciably due to the presence of a groove separating the source and the drain regions; and consequentially their respective depletion regions. Further integration of concave MOSFETs with dual material gate architecture [6-7] enhances the driving current capability and suppresses the short channel effects. The resultant integrated device structure is referred to as L-DUMGAC MOSFET [8-9].

This work focuses on the TCAD assessment of L-DUMGAC MOSFET for high performance RF applications in terms of RF figure of merits such as stern stability factor, maximum available power gain and intrinsic delay. Further, the impact of various technological variations such as gate length and negative junction depth (NJD) is explored on these device metrics for improved performance. All simulations have been performed using ATLAS [10] device simulation software. The models activated in simulation comprise the inversion layer Lombardi CVT mobility model along with Shockley–Read–Hall (SRH) and Auger recombination model for minority carrier recombination.

2 SIMULATION RESULTS AND DISCUSSION

Maximum available power gain (Gma) and stability are two of the most important considerations for use in Low Noise Amplifier (LNA) and RF amplifier design.

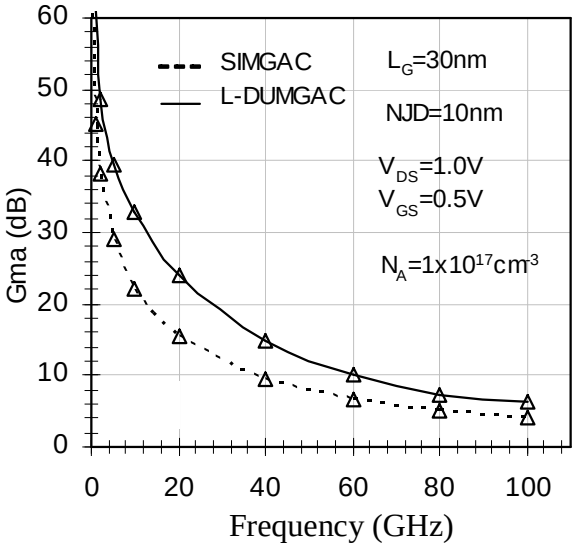

Figure 1: Maximum Available Power Gain, Gma, for SIMGAC & L-DUMGAC MOSFET designs.

Fig.1 reflects the performance enhancement of L-DUMGAC in terms of Gma which indicates the maximum theoretical power gain that can be expected from the device. Improvement in Gma is experienced with L-DUMGAC due to lower parasitics and improved gate control.

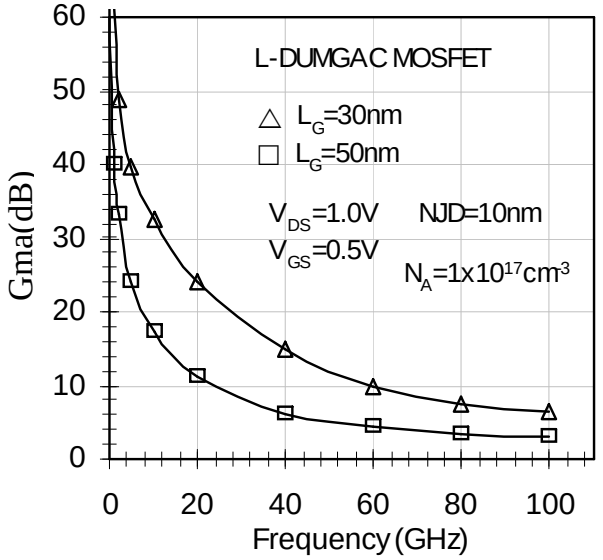

Figure 2: Maximum Available Power Gain, Gma, for L-DUMGAC MOSFET design giving L_G variation.

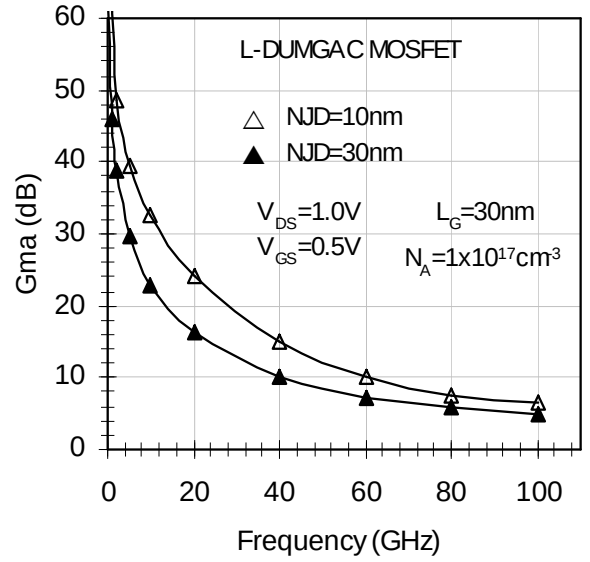

Figure 3: Maximum Available Power Gain, Gma, for L-DUMGAC MOSFET design giving NJD variation.

As the gate length is reduced, the performance metrics further enhance, owing to improved drive current as is depicted from Fig.2. Further, from Fig.3, it is reflected that reduction in NJD also leads to the power gain improvement as a result of higher gate control over the channel. Fig.4 explains the stability of L-DUMGAC and conventional SIMGAC MOSFETs.

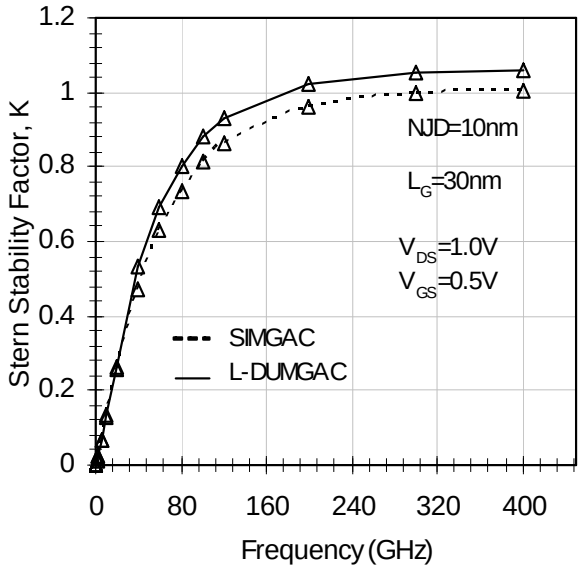

Figure 4: Stern Stability Factor, K, for SIMGAC & L-DUMGAC MOSFET designs.

The Stern Stability Factor (K) predicts the absolute stability of a transistor and is usually less than 1 (i.e. unstable) at LF and higher than 1 (i.e. stable) at HF. As is clear from the figure, K is appreciably higher (or greater than 1), for L-DUMGAC in comparison to SIMGAC where K is just approaching 1; reflecting an oscillatory nature of SIMGAC MOSFET. If K is less than 1, the circuit is potentially unstable and a simultaneous input and output impedance match cannot be obtained for maximum power transfer.

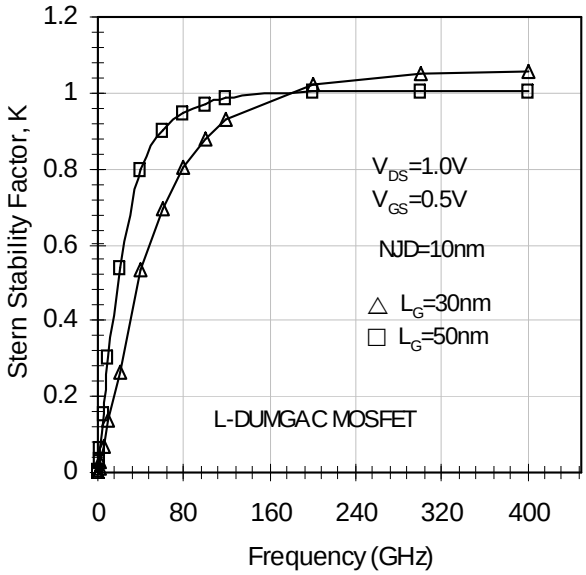

Figure 5: Stern Stability Factor, K, for L-DUMGAC MOSFET design giving L_G variation.

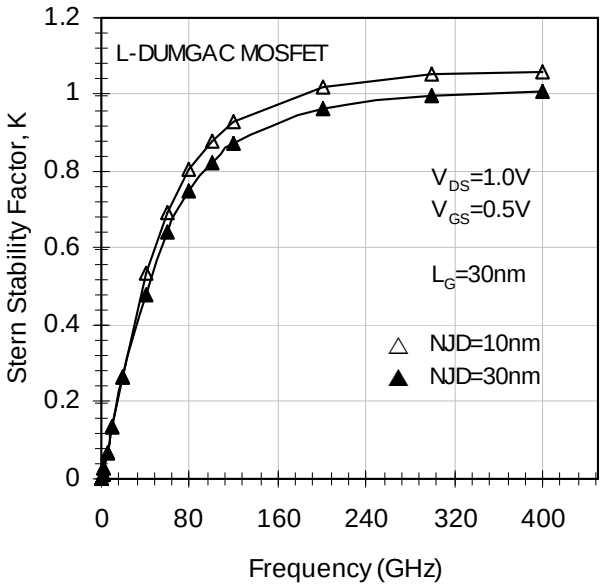

Figure 6: Stern Stability Factor, K, for L-DUMGAC MOSFET design giving NJD variation.

However, if K is greater than 1, the circuit is stable, thereby maximizing the power transfer. Device miniaturization, however, leads to instability, as is predicted from Fig.5, owing to reduced gate control as a result of overlapping of the source and drain fields in the scaled devices. Further, Fig.6 reflects that NJD reduction perks up the K-factor. This is due to increased gate controllability of the device over the channel which hence, results in the maximum power transfer from source to load. Fig.7 compares the SIMGAC and L-DUMGAC devices using the intrinsic delay metric. Intrinsic delay of the L-DUMGAC structure is significantly lower than the SIMGAC MOSFET i.e. incorporation of the DMG architecture leads to an appreciable reduction of intrinsic delay by 63.8%. Further, increase in the gate length intensifies the intrinsic delay resulting in device switching

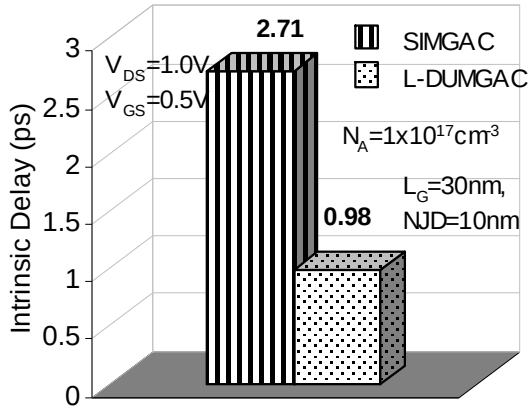

Figure 7: Intrinsic Delay Metric Evaluation for SIMGAC & L-DUMGAC MOSFET designs.

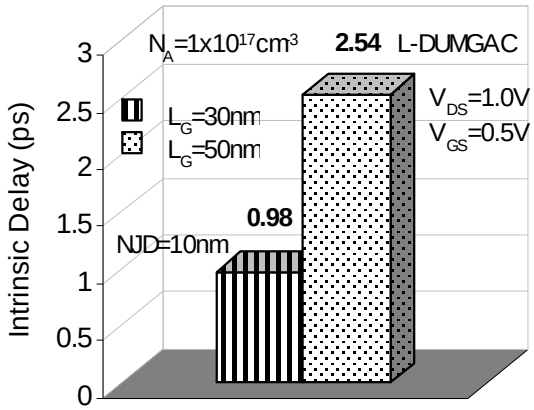

Figure 8: Intrinsic Delay Metric Evaluation for L-DUMGAC MOSFET design giving L_G variation.

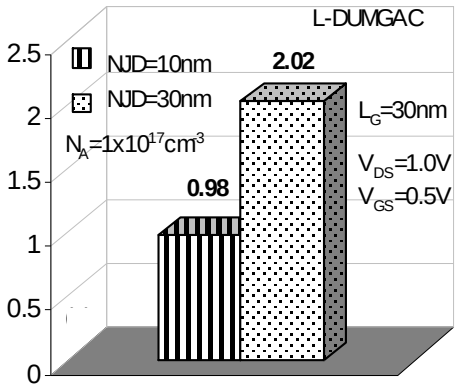

Figure 9: Intrinsic Delay Metric Evaluation for L-DUMGAC MOSFET design giving NJD variation.

deterioration as is clear from Fig.8. Moreover, with decrease in NJD from 30nm to 10nm, the intrinsic delay improves by 51.4% for L_G=30nm as demonstrated in Fig.9. This is mainly due to the decrease in potential barriers at the corners leading to enhanced carrier transport. Thus, L-DUMGAC leads to a decrease in the parasitic behavior resulting in high speed performance and, hence, proves to be a promising candidate in terms of switching speed.

3 CONCLUSION

In this paper, we have systematically investigated the effect of dual material gate architecture on the concave MOSFET for improved transistor RF performance. It has been observed that L-DUMGAC device exhibits significantly improved power gain with an appreciably low intrinsic delay; hence, proving its effectiveness in RF/wireless applications. Moreover, L-DUMGAC MOSFET is found to be more stable than the SIMGAC MOSFET; reflecting improved gate controllability and

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maximum power transfer from source to load. These results therefore show the potential of L-DUMGAC technology for low noise, high-performance System-On-Chip and RF applications.

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