Compact Analytical Threshold Voltage Model for Nanoscale Multi-Layered-Gate Electrode Workfunction Engineered Recessed Channel (MLGEWE-RC) MOSFET

R.Chaujar*, R.Kaur*, M.Saxena**, M.Gupta* and R.S.Gupta*

* Semiconductor Devices Research Laboratory, Department of Electronic Science, University of Delhi, South Campus, New Delhi, India, rishuchaujar@rediffmail.com and ravneetsawhney13@rediffmail.com, rsgu@bol.net.in

**Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, Karampura, New Delhi, India, saxena_manoj77@yahoo.co.in

ABSTRACT

In this paper, a compact analytical threshold voltage model for multi-layered-gate electrode workfunction engineered recessed channel (MLGEWE-RC) MOSFET is presented and investigated using ATLAS device simulator. The novel device integrates the merits of recessed channel, gate electrode workfunction engineered (GEWE) architecture and multi-layered gate dielectric design. Our model includes the evaluation of surface potential, electric field distribution along the channel and threshold voltage. We demonstrate that MLGEWE-RC MOSFET design exhibits significant enhancement in terms of improved hot carrier effect immunity, carrier transport efficiency and reduced short channel effects (SCEs) proving its efficacy for high-speed integration circuits and analog design. The accuracy of the results obtained using our analytical model is verified using 2-D device simulations.

Keywords: ATLAS, high-K, MLGEWE-RC, surface potential and threshold voltage.

1 INTRODUCTION

For the last few decades, Si CMOS technology has been driven by device scaling to increase performance, as well as reduce cost and maintain low power consumption. With scaling of the device dimensions into the sub-100-nm regime, the gate oxide thickness of CMOS transistors has also been scaled down constantly. As continual CMOS scaling requirements and many digital and mixed-signal applications are driven by standby power consumption, the gate leakage current is becoming one of the critical elements of sub-65 nm CMOS technology development. A paradigm shift has been occurring in the industry, where materials innovation, rather than scaling, is becoming the primary enabler for performance enhancement in CMOS technology. For gate materials, traditional SiO_2 is being replaced by high-K dielectrics to reduce the gate leakage current.

A high-K gate dielectric becomes a key in providing the increased physical gate dielectric thickness, $t_{ox}(=t_{ox1}+t_{ox2})$, keeping effective oxide thickness (t_{oxeff}) same; without compromising the direct tunneling gate leakage current. Increasing physical gate dielectric thickness, however, results in a higher gate-fringing field, thereby reducing the gate control and hence, aggravating short channel effects (SCEs) [1-2]. An ultra thin SiO_2 interlayer between the high-K layer and silicon substrate is, thus, introduced, in order to improve the interface quality and stability. The CMOS transistors designed with the multi-layered high-k gate dielectrics achieve the expected high drive current performance and lower leakage current, thereby proving its efficacy for high performance CMOS logic applications.

Recessed Channel (RC) MOSFETs [3-4] are known to alleviate the short channel effects and the hot carrier effects appreciably due to the presence of a groove separating the source and the drain regions; and consequentially their respective depletion regions. Further integration of RC MOSFETs with dual material gate architecture [5-6] and multi-layered gate dielectric architecture enhances the driving current capability, gate control over the channel and suppresses the short channel effects. The resultant integrated device structure is, thus, referred to as MLGEWE-RC MOSFET.

The primary objective here is to apply the dual gate material architecture and multi-layered gate dielectric concept to RC MOSFET and explain the unique features offered by this structure. An analytical model using Poisson's equation has also been presented for the surface potential, electric field and threshold model for the MLGEWE-RC MOSFET and its validation is done with ATLAS device simulation results [7]. A very close match has been found between the model and simulation results. The results are then compared with the conventional RC and GEWE-RC MOSFET designs; reflecting enhancement in device characteristics of the proposed MLGEWE-RC MOSFET design.

2 MODEL FORMULATION

A schematic structure of MLGEWE-RC MOSFET is shown in Fig.1 with M_1 and M_2 of lengths L_{g1} and L_{g2} respectively. In MLGEWE-RC MOSFET, the gate consists of multi-layered-gate dielectrics having a thickness t_{ox1} and t_{ox2} of the lower and the upper gate dielectrics with the corresponding permittivites, ε_{ox1} and ε_{ox2}, respectively. The

source/drain (S/D) regions are rectangular and uniformly doped at 10^{20} cm^{-3}. The channel doping concentration (or substrate doping density), N_A, is also uniform. Assuming the impurity density in the channel region to be uniform, the potential distribution $\zeta(x, y)$ in silicon film in the weak inversion region can be given as

$$\frac{\partial^2 \zeta(x, y)}{\partial x^2} + \frac{\partial^2 \zeta(x, y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}};$$

for $0 \le x \le L_{eff}$ and $(d + t_{oxeff}) \le y \le (d + t_{oxeff} + Y_D)$ (1)

where ε_{si} is the dielectric constant of silicon, q is the electronic charge, Y_D is the depletion layer thickness, t_{oxeff} is the effective gate oxide thickness ($=t_{ox1}+(\varepsilon_{ox1}/\varepsilon_{ox2})t_{ox2}$), d is the groove depth and L_{eff} is the effective channel length which is given by,

$$L_{eff}=L_g+2(t_{oxeff}+NJD) \quad (2)$$

where L_g is the gate length ($L_g=L_{g1}+L_{g2}$); NJD is the negative junction depth and Y_D is the depletion layer thickness.

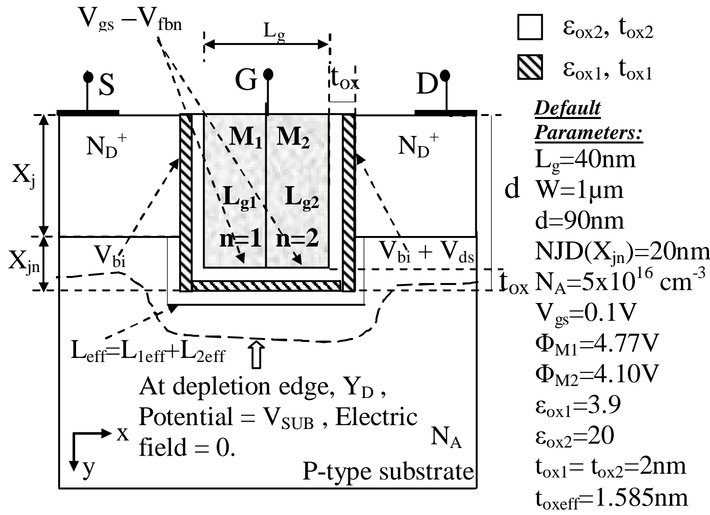

Figure 1: Schematic cross-section of MLGEWE-RC MOSFET design.

In the present analysis, the channel region has been divided into two parts, in which the potential under M_1 and M_2 can be represented as

$$\zeta_1(x, y) = \zeta_{S1}(x, d + t_{oxeff}) + \sum_{r=1}^{3} P_{r1}(x)\, y^r$$

for $0 < x \le L_{1eff}$; $(d + t_{oxeff}) \le y \le (d + t_{oxeff} + Y_D)$ (3)

$$\zeta_2(x, y) = \zeta_{S2}(x, d + t_{oxeff}) + \sum_{r=1}^{3} P_{r2}(x)\, y^r$$

for $L_{1eff} < x \le (L_{1eff} + L_{2eff})$;$(d + t_{oxeff}) \le y \le (d + t_{oxeff} + Y_D)$ (4)

where

$$L_{1eff} = L_{g1} + (NJD + t_{oxeff}); \quad L_{2eff} = L_{g2} + (NJD + t_{oxeff})$$

$\zeta_1(x, y) = \zeta_{S1}(x, d + t_{oxeff})$ and $\zeta_2(x, y) = \zeta_{S2}(x, d + t_{oxeff})$ are surface potentials under regions M_1 and M_2, and $P_{r1}(x)$ and $P_{r2}(x)$ are the arbitrary coefficients. The Poisson equation is solved separately under the two regions (M_1 and M_2) using the boundary conditions shown in Fig.1. Further, substituting $\zeta_{S1}(x_{min}, d + t_{oxeff}) = 2\zeta_f$ *and* $V_{gs} = V_{th}$ in the expression for minimum surface potential, an expression for threshold voltage is obtained as

$$V_{TH} = \frac{2\zeta_F + \left[\frac{qN_A}{\varepsilon_{si}} + \left(\frac{2Y_D^2 + 8dY_D + 8t_{oxeff}Y_D - 8(\alpha)}{(\alpha)^2(\beta)}\right)\cdot V_{SUB}\right]\cdot\lambda^2 - \delta_1(x_{min})}{1 + \left(\frac{2Y_D^2 + 8dY_D + 8t_{oxeff}Y_D - 8(\alpha)}{(\alpha)^2(\beta)}\right)\cdot\lambda^2} + V_{FB1} \quad (5)$$

3 RESULTS AND DICUSSION

Fig. 2 reflects a higher step near the drain end for the proposed MLGEWE-RC MOSFET design in comparison to the other two designs, thus resulting in better screening of the channel region from drain bias variations.

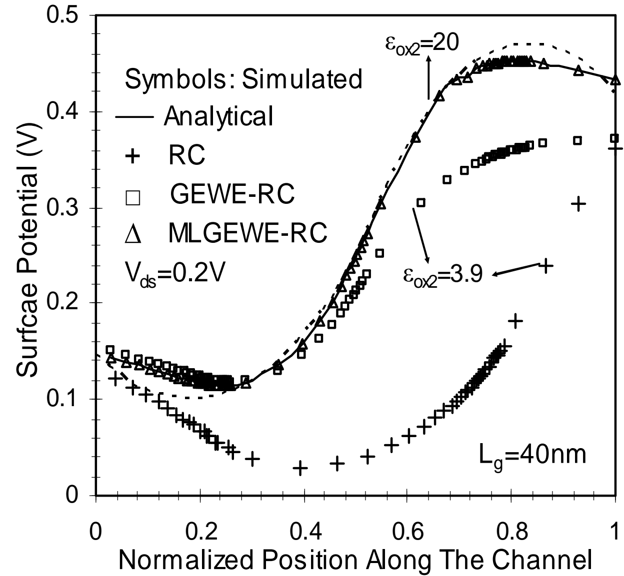

Figure 2: Surface potential variation with the normalized channel position comparing 3 different designs.

NSTI-Nanotech 2008, www.nsti.org, ISBN 978-1-4200-8505-1 Vol. 3

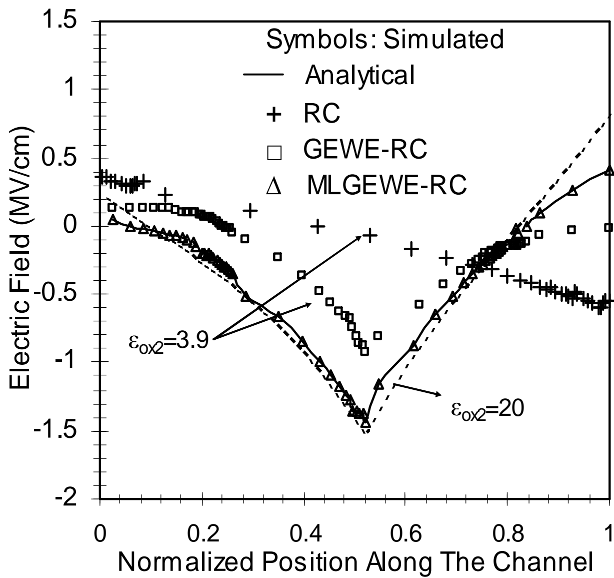

Figure 3: Electric Field variation with the normalized channel position comparing 3 different designs.

Further, the lateral field penetration from Source/Drain region is reduced significantly due to the recessed gate nature of the device, minimizing the DIBL and punchthrough effects. This lateral penetration of the field is further reduced with the use of gate stack, as is evident from Fig.3. Results reflect a higher electric field peak, for the proposed design, at the interface of two metal gates; thus causing more uniformity of electric field in the channel. This, hence, results in higher carrier transport efficiency. Further, Fig.4 reflects that V_{TH} reduces as upper gate oxide permittivity increases, thereby, enhancing the drive current.

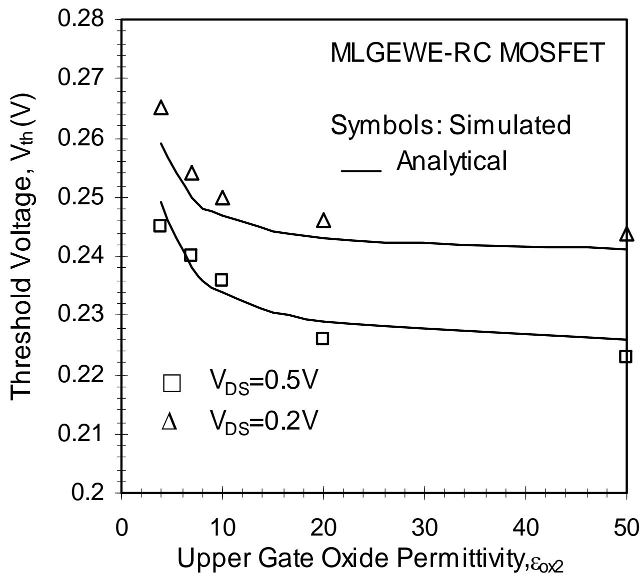

Figure 4: Threshold voltage variation as a function of upper gate oxide permittivity for 2 different drain bias.

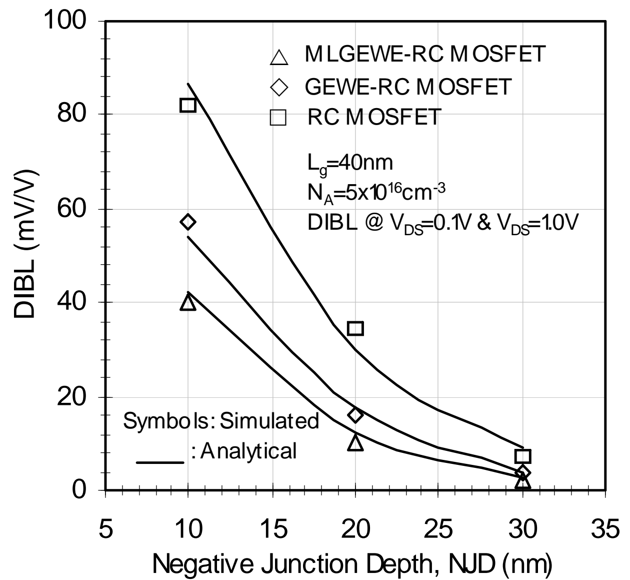

Figure 5: DIBL variation with negative junction depth, NJD, for RC, GEWE and MLGEWE-RC MOSFETs.

Fig.5 depicts that MLGEWE-RC exhibits the minimum DIBL due to the step potential profile, attributed to GEWE architecture and improved gate control over the channel, attributed to the multi-layered gate oxide architecture. Further, higher the negative junction depth (NJD), better is the screening of the channel region from the drain bias variations. It is seen that MLGEWE-RC MOSFET exhibits significant enhancement in terms improved gate control over the channel, carrier transport efficiency and hence, the driving current and hot carrier effect immunity.

4 CONCLUSION

The effectiveness of the GEWE and multi-layered gate dielectric concept to the RC structure has been examined for the first time by developing a 2-D analytical model. The results obtained have been compared with ATLAS simulations. The model results agree well with the simulated results. It also emphasizes that the proposed structure improves gate controllability over the channel and further leads to a reduced short channel effects as the surface potential profile shows a step at the interface of the two metals. Thus the short channel behavior of the RC MOSFETs is further enhanced with the introduction of the GEWE and gate stack structure over their single gate counterparts.

5 ACKNOWLEDGMENTS

Authors are grateful to Defense Research and Development Organization (DRDO), Ministry of Defense, Government of India, and one of the authors (Rishu Chaujar) is grateful to University Grant Commission (UGC) for providing the necessary financial assistance to carry out this research work.

REFERENCES

[1] B.Cheng, M.Cao, R.Rao, A.Inani, P.V.Voorde, W.M.Greene, et.al, “The Impact of High-k Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFET’s”, IEEE Trans. Electron Devices, 46, 1537-1544, 1999.

[2] R.Chau, S.Datta, M.Doczy, B.Doyle, J.Kavalieros and M.Metz, “High-k/Metal-Gate Stack and Its MOSFET Characteristics”, IEEE Elect. Device Lett., 25, 408-410, 2004.

[3] P.H.Bricout and E.Dubois, “Short-Channel Effect Immunity and Current Capability of Sub-0.1-Micron MOSFET’s Using a Recessed Channel”, IEEE Trans. Electron Devices, 43, 1251-1255,1996.

[4] H.Ren and Y.Hao, “The influence of geometric structure on the hot-carrier-effect immunity for deep-sub-micron grooved gate PMOSFET”, Solid-State Electronics, 46, 665-673, 2002.

[5] W.Long, H.Ou, J.M.Kuo and K.K.Chin, “Dual-Material Gate (DMG) Field Effect Transistor”, IEEE Trans. Electron Devices, 46, 865-70, 1999.

[6] X.Zhou, “Exploring the novel characteristics of hetero-material gate field-effect transistors (HMGFET’s) with gate-material engineering,” IEEE Trans. Electron Devices, 47, 113–120, 2000.

[7] ATLAS: Device simulation software, 2002.