Synthesis and Characterization of Ni/Si Nanowires for Electrical Transport

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ABSTRACT

Self-assembled Si nanowires (SiNWs) have been synthesized and characterized as a template for surface metal silicide formation to investigate confinement of electron transport at the nanowire surface. The SiNWs with diameters ranging from 5 to 180 nm were synthesized via the solid-liquid-solid (SLS) mechanism with a sputtered Au film as catalyst. Post-deposition thermal processing was carried out for silicide formation. Metal-silicide coated wires were dispensed on metal-patterned Si wafers to carry out two-point and four-point electrical conductivity measurements. Electrical contacts were formed via FIB-based Pt deposition. Metal-silicide-coated SiNWs exhibited an improvement in electrical conductivity of several orders of magnitude. Preliminary analyses imply variable thickness of the metal silicide region based, in part, on deposition methodology and thermal process parameters.

Keywords: silicon nanowire (SiNW), solid-liquid-solid (SLS), nickel silicide, electrical conductivity

1 INTRODUCTION

Semiconductor and metallic nanowires have attracted substantial attention for a variety of nanoelectronic applications. In particular, silicon nanowires (SiNWs) may be an attractive alternative to conventionally processed Si transistors if their intrinsic self-assembly can be harnessed to obviate the need for complex lithographic techniques for device fabrication. In addition, SiNWs can potentially function as both the switch (i.e. transistor) and local interconnect (e.g. metal silicide nanowire) to form an inherently integrated nanoelectronic system – potentially on the same self-assembled nanostructure [1-3].

In terms of metal silicide candidates for such nanostructures, nickel silicide (NiSi) possesses several advantages including low resistivity and low formation temperature [4-7]. In fact, for current CMOS technology NiSi has been shown to be a good electrical contact material for gate, source and drain [8-10]. Recent demonstrations of excellent conductance in NiSi nanowires have also highlighted the excellent potential for SiNW-based systems.

Currently, there are several methods available to synthesize silicon nanowires including laser ablation [1, 11], physical vapor deposition [12], thermal evaporation [13], chemical vapor deposition [14-16], solid-liquid-solid (SLS) growth [17, 18], vapor-liquid-solid (VLS) growth [19, 20], and oxide assisted growth [21]. The SLS growth is a relatively straightforward technique to synthesize nanowires without a gas phase precursor such as SiH_4 or $SiCl_4$. Via the SLS process, silicon nanowires can be directly grown on a silicon substrate which acts as the silicon [17].

In the SLS process, a thin metal film is deposited on a single-crystal silicon substrate (e.g. (100) Si wafer) as a catalyst. Heating of the metallized Si results in metal droplet formation. Continuous diffusion of silicon atoms from the substrate to the droplet at elevated temperatures causes saturation of silicon inside the droplet, and subsequent precipitation at the surface of the droplet. In the presence of a negative temperature gradient at the droplet surface (e.g. due to a gas flow) the surface Si precipitate forms a Si growth front resulting in nanowire formation from the catalyst [17].

In this paper, we report investigations of SLS-grown SiNWs as templates for the surface formation of NiSi to investigate confinement of electron transport at the nanowire surface. Silicon nanowires were grown via the SLS approach on Si (100) and (111) substrates using a sputtered Au film as catalyst in an oxygen-filtered Ar ambient. The influence of annealing time on SLS SiNW growth is discussed in term of nanowire diameter. Post-growth Ni deposition is followed by variable-rate thermal processing to investigate the surface morphology of nickel silicide formation.

Following thermal processing, NiSi-coated SiNWs underwent electrical conductivity testing within two-point and four-point probe structures processed within a focused ion-beam scanning electron microscope (FIB-SEM).

2 EXPERIMENTAL DETAILS

The substrates used were p-type (100) and (111) silicon wafers with electrical resistivity in the 1-10 Ω•cm range. Wafers were cleaned with diluted hydrofluoric acid (1%) to remove the native oxide layer and ultrasonicated in acetone to remove organic contamination. The cleaned samples were immediately loaded into a PVD (evacuated to 5×10^{-7} Torr) for sputtering of a 4 nm thick Au catalyst film.

Following Au deposition the silicon samples were placed inside an annealing chamber. The annealing chamber was evacuated to a base pressure of approximately 5 Torr and backfilled with high purity (99.999%) Ar. In order to reduce residual oxygen in the chamber an oxygen filter and a bypass line were configured in the Ar supply.

The total pressure of the system was then raised to atmospheric pressure. The Au/Si sample was annealed at 1000 °C (30 minute ramping time) under Argon (99.999% purity) gas flow at 2,000 sccm. The annealing duration after the temperature ramp was varied from 10 minutes to 120 minutes to investigate the effect of annealing time on the nanowire diameter, length, and overall morphology.

Ni deposition and subsequent thermal processing was carried on as-deposited SLS SiNWs to investigate surface silicide formation. Nickel was deposited on the nanowires via e-beam evaporation (calibrated for an effective blanket film thickness of 150 nm). Nickel deposited SiNW samples were annealed using a rapid thermal annealing system at 550 °C for 5 min and at 600 °C for 5 min with 10 min ramping time to compare resultant SiNW morphologies which were investigated by SEM.

Metal-coated SiNWs and as-grown SiNWs were dispensed on metal-patterned Si wafers to carry out two-point and four-point electrical conductivity measurements. Electrical contacts were formed using Pt deposition within a dual beam FIB-SEM. Structural and compositional properties of these wires were analyzed using SEM, energy dispersive x-ray spectroscopy (EDS), and transmission electron microscopy (TEM).

3 RESULTS

The solid-liquid-solid (SLS) method, as described above, was used to synthesize silicon nanowires. The samples were taken out of the annealing furnace after cooling to room temperature. The effects of annealing duration were investigated. The furnace temperature was ramped up to 1,000 °C for 30 min under 2,000 sccm of Ar flow. After the ramp the furnace temperature was held constant for durations ranging from 10 minutes to 120 minutes. Figure 1 shows SEM micrographs of typical SiNWs synthesized for various anneals (1000 °C). An approximately bimodal diameter distribution was observed. Increased annealing time resulted in larger SiNW diameters. SiNWs diameters ranged from 5-22 nm after 10 minute annealing, 45-52 nm after 60 minute annealing, and 77-180 nm after 120 minute annealing.

Si nanowires exhibiting the smallest diameters of 5 nm observed here have not been reported previously (grown via SLS). Typically, small diameter nanowires were only reported for vapor-liquid-solid (VLS) growth when utilizing nm-thick catalyst layers or distributions of nm-scale catalytic particles. In VLS growth, controlling the diameter of nanowires can be achieved by adjusting the precursor and pressure. However, in conventional SLS growth, diameter control is a challenge since SiNW growth is proceeds rapidly at high temperature. In the work reported here, variation of the anneal duration and Ar gas flow rate serve to immediately quench the growth and help regulate SiNW diameter.

After growth, SiNWs were detached from the initial silicon wafer using ultrasonication in a solvent and distributed on highly oriented pyrolytic graphite (HOPG) substrates to carry out compositional analyses.

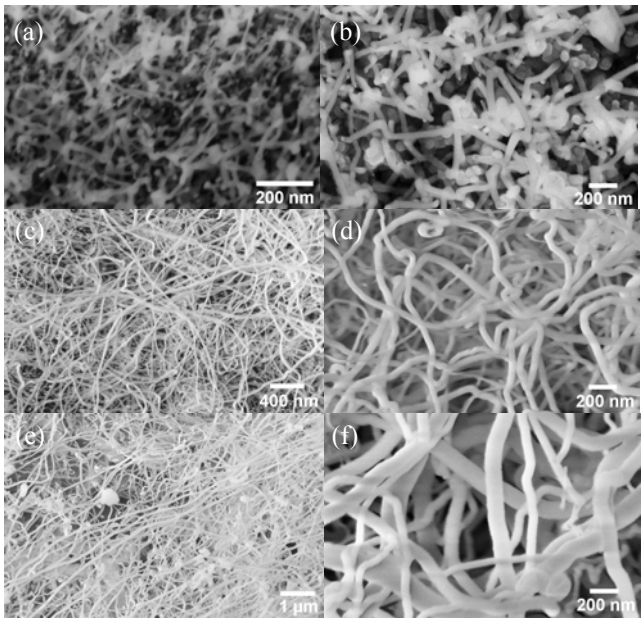

Figure 1: SEM micrograph of nanowires synthesized at 1000 °C for (a) 10 min, (b) 15 min, (c) 45 min, (d) 60 min, (e) 90 min, (f) 120 min annealing times. Deposited Au catalyst layer was 4 nm thick.

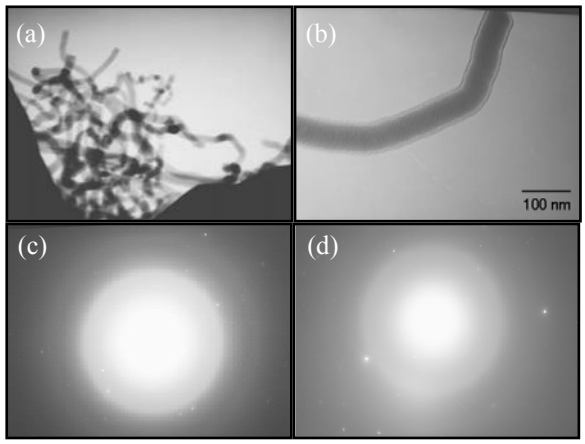

Figure 2: (a) TEM micrograph showing the morphology of a SiNW bundle, (b) Single SiNW, (c), (d) Selected-area electron diffraction (SAED) patterns from SiNWs.

Selected-area electron diffraction (SAED) patterns (Fig. 2(c) and 2(d)) were acquired from individual SiNWs. These implied an amorphous microstructure for the SiNWs evaluated. This implies the possible presence of oxygen in the SiNWs. It should be noted that crystalline nanowires have been typically observed via VLS growth, while SLS methods generally produce amorphous nanowires. This may be due to the fast growth rate and high temperature of the SLS process, which leads to amorphous rather than crystalline growth.

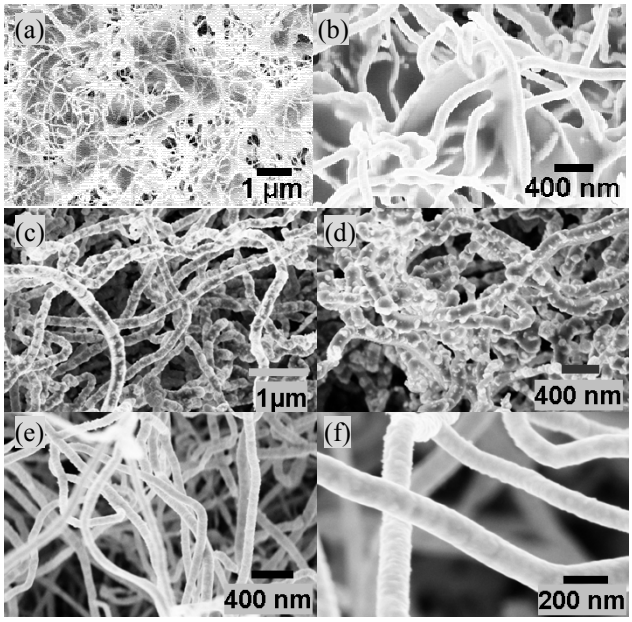

Figure 3: SEM images of Ni-deposited SiNWs: (a), (b) as-deposited; (c), (d) Ni-deposited SiNW after slow annealing at 600 °C for 10 minutes in Ar ambient (c), (d). Note rough surface morphology; (e), (f) Ni-deposited SiNW after rapid thermal annealing at 550 °C for 5 minutes in N_2 ambient. Note smooth morphology.

Nickel was deposited on the nanowires by e-beam evaporation calibrated for an effective blanket film thickness of 150 nm. Post-deposition thermal processing was carried out for nickel silicide formation (550 °C for 5 minutes via RTA and 600 °C for 5 minutes with a 10 minute ramp). Post-anneal nanowire surface morphology was sensitive to anneal temperature and ramp rate. Rapid ramps resulted in an atomically-smooth Ni-SiNW template morphology. Slow annealing resulted in a rough Ni-SiNW surface morphology indicative of nonuniform silicide domain formation, as shown in Fig. 3.

Energy dispersive x-ray spectroscopy (EDS) was performed for post-annealed Ni-deposited SiNWs on an HOPG substrate for compositional analysis. Figure 4 shows EDS spectra of nanowires on the initial silicon substrate, after Ni deposition, after slow annealing, and after RTA (the latter three on HOPG substrates). The results confirm the presence of nickel on individual SiNWs after thermal processing. Note the substantial increase of the La peak (0.85 keV) relative to the Ka peak (7.47 keV) for the annealed Ni-SiNWs. This implies nickel silicide formation [6, 22, 23]. The EDS data in Fig. 4 also confirm the presence of oxygen in the SiNWs.

As-grown silicon nanowires and metal-silicide coated SiNWs were dispensed on SiO_2-coated Si wafers patterned with a metal (Au) electrode pattern to carry out electrical conductivity measurements. Electrical connection between the dispensed SiNWs and the Au electrodes were formed via direct-write FIB-based Pt deposition. Figures 5a and 5b show an SEM micrograph and associated current-voltage characteristic of an as-grown SiNW, respectively. The I-V response of the SiNW is linear and the two-point resistivity of similar SiNWs ranged from 20 Ω·cm to 2×10^5 Ω·cm. The observed electrical resistivity range for as-deposited SiNWs rules out a dominant SiO_2 stoichiometry, although it is not inconsistent with local SiO_x compositions within the nanowire. (No current measurement was possible for open Pt electrodes confirming the insulative properties of the SiO_2 dielectric in the electrical test structure.)

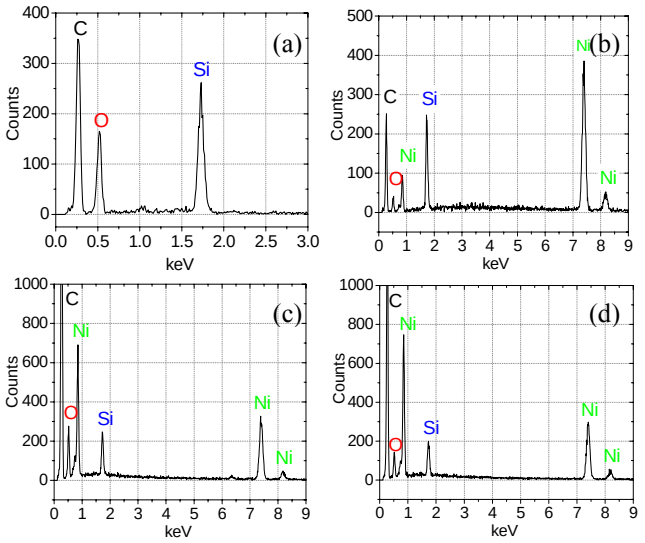

Figure 4: EDS spectra of nanowires: (a) as-grown nanowire on the initial silicon substrate; (b) after Ni deposition (on HOPG); (c) after slow annealing (on HOPG); (d) after rapid annealing (on HOPG).

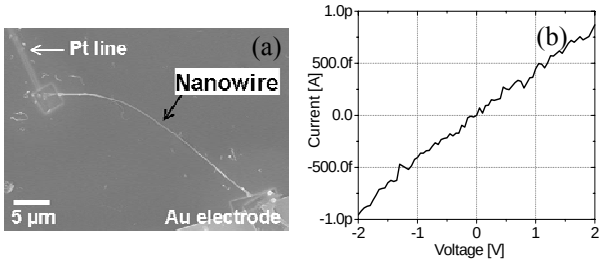

Figure 5: Pt deposition and I-V measurement of dispensed as-grown silicon nanowire. (a) SEM image of the wire connected by Pt lines on Au-patterned oxide substrate, nanowire length was 29 µm and diameter was 168 nm. (b) I-V characteristics.

The resistivity of post-annealed Ni-SiNW wires was measured by two- and four-point electrical conductivity measurements, as shown in Fig. 6. Two- (Fig. 6a) and four- (Fig. 6c) point I-V measurements yield resistance of 2 MΩ and 55 kΩ, respectively, for the 9.2 µm long device with a diameter of 165 nm, which corresponds to a resistivity of 0.47 Ω·cm and 0.013 Ω·cm, respectively.

Fig. 6 (d) shows calculated resistivity from as-grown nanowires and metal-silicide coated wires. It is clear that after post-deposition of nickel on the silicon nanowires the conductivity is increased up to 7 orders.

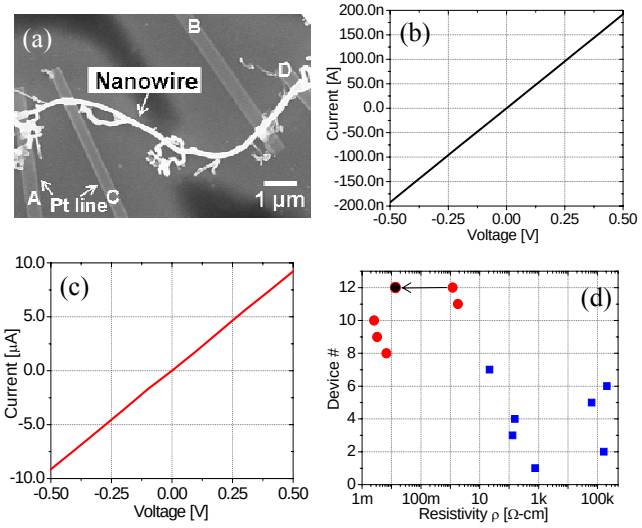

Figure 6: (a) SEM image of metal-silicide coated wire with four terminals, (b) I-V characteristics via two-point measurement, (c) via four-point measurement, (d) calculated resistivity from as-grown nanowires (blue squares) and metal-silicide coated wires (red circles).

4 CONCLUSION

Self-assembled Si nanowires were synthesized and characterized as a template for surface metal silicide formation to investigate confinement of electron transport at the nanowire surface. Silicon nanowires with diameters ranging from 5 to 180 nm were synthesized via solid-liquid-solid (SLS) growth. The diameter of as-grown SiNWs can be controlled, to an extent, through the annealing time.

Post-growth Ni deposition and thermal processing was carried out for nickel silicide formation at the SiNW surface. Post-annealed Ni-SiNW surface morphology was sensitive to anneal temperature and ramp rate. Rapid ramps resulted in an atomically smooth Ni-SiNW surface morphology. Slow annealing resulted in a rough Ni-SiNW surface morphology indicative of nonuniform domain formation. EDS measurements confirm that the nickel remains on the SiNW surface after thermal processing. Also, the substantial increase of the La peak (0.85keV) relative to the Ka peak (7.47 keV) in the EDS spectra for the annealed Ni-SiNWs implies nickel silicide formation.

Metal-silicide coated wires were dispensed on metal-patterned Si wafers to carry out two-point and four-point electrical conductivity measurements. Electrical contacts were formed via FIB-based Pt deposition. Metal-silicide-coated SiNWs exhibited an improvement in electrical conductivity of several orders of magnitude compared with that of as-grown silicon nanowires.

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