Structure Generation for the Numerical Simulation of Nano-Scaled MOSFETs

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ABSTRACT

An accurate and predictive numerical simulation of MOS transistors in the deca-nanometer channel length regime relies on the precise mapping of the physical device to a simulation model. A quick and accurate method which allows to extract the relevant transistor parameters, based on data which are typically available within a process flow, is presented.

Keywords: MOSFETs, TCAD, numerical device simulation

1 INTRODUCTION

To make TCAD analysis applicable to state-of-the-art MOSFETs in the deca-nanometer channel length regime [1], numerical simulation using advanced transport models [2] is required. An accurate and predictive result relies on the precise mapping of the physical device onto a virtual structure. Besides the use of full process simulation, which requires extensive calibration of the underlying models, this work presents an alternative approach for the quick estimation of the relevant device parameters.

2 STRUCTURE GENERATION

We developed a method to setup simulations with the data available during the production with the aim to assist the device engineer. The topological structure of the devices is directly extracted from TEM images, which are available for each major process step. In contrast to simple template device structures, the full transistor geometry is covered. A device editor allows to identify the device regions and to create the segments as shown in Fig. 1. The doping profiles can be specified using analytical distribution functions or numerically, provided from previously obtained calibrated process simulation or from SIMS measurements (c.f. Fig. 2).

3 GRID GENERATION

The grids for the numerical solution of the PDE system are generated automatically using a basic triangulation of the regions and a quad tree refinement strategy [3]. A segment is divided into four rectangular sub regions. If the quality criterion is not met, a sub region is recursively refined until sufficent accuracy is achieved. This is demonstrated in Fig. 3.

For MOSFETs, two criteria apply: The channel refinement follows the distance to the interface in order to properly resolve the inversion channel. The junction refinement depends on the gradient of the dopant concentrations. This ensures accurate simulation results and good convergence [4]. Simulation grids with the applied refinements are shown in Fig. 4.

4 SIMULATION MODELS

A pMOS transistor is considered. For holes, the energy transport model has been applied:

$$\begin{aligned}
\mathbf{J}_p &= -\mu_p \mathrm{k_B} \left(\nabla \left(p T_p \right) - \frac{\mathrm{q}}{\mathrm{k_B}} \mathbf{E} p \right) \,, \\
\mathbf{S}_p &= -\frac{\tau_S}{\tau_m} \left(\frac{5 {\mathrm{k_B}}^2}{2\mathrm{q}} \mu_p p T_p \nabla T_p - \frac{5 {\mathrm{k_B}}^2}{2\mathrm{q}} T_n \mathbf{J}_p \right) \,, \\
\nabla \cdot \mathbf{J}_p &= -\mathrm{q} R \,, \\
\nabla \cdot \mathbf{S}_p &= \mathbf{E} \cdot \mathbf{J}_p - \frac{3}{2} \mathrm{k_B} p \frac{\mathrm{T}_p - T_L}{\tau_{\mathcal{E}}} - G_{\mathcal{E}p} \,.
\end{aligned}$$

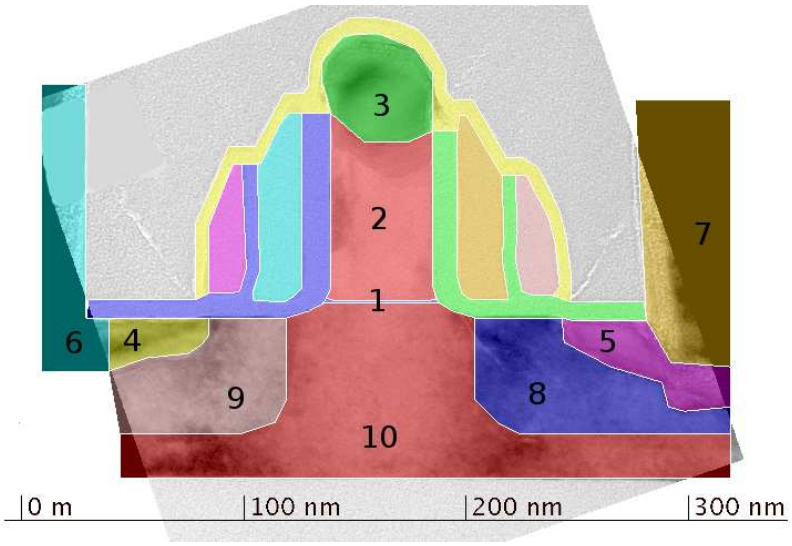
Here, $\mathbf{S}$ denotes the energy flux density, T_p the local hole temperature, $\tau_{\mathcal{E}}$, τ_S, and τ_m the energy, energy flux, and momentum relaxation time, respectively, and $G_{\mathcal{E}p}$ the net energy generation rate [2].

The electrons are treated within a quasi-fermi level (QFL) approximation. For the simulation of the partially depleted SOI MOSFET, a combined QFL scheme was applied [6]. It typically converges within a few iterations for the biased device.

The gate leakage current is calculated within a post processing step by evaluation of the Tsu-Esaki formula [7].

5 RESULTS AND CONCLUSION

The described methodology has been used to investigate a state-of-the-art pMOS transistor fabricated on SOI substrate [5]. Based on a TEM image the material properties are assigned, the dopant profile is defined, and a numerical analysis of the device has been carried out. This allows to inspect distributed quantities like



Nr	Name	Material
1	Oxide	SiO_2
2	Gate	Poly-Si
3	GateContact	Silicide
4	SourceContact	Silicide
5	DrainContact	Silicide
6	SourceContact2	Metal
7	DrainContact2	Metal
8	Drain	SiGe
9	Source	SiGe
10	Bulk	Si

Figure 1: The topological structure of the device is directly created from a TEM-image using the segment editor. The silicide regions (4 and 5) have been modeled as conductors. The SiGe regions have a Ge content of 20 %. [5]

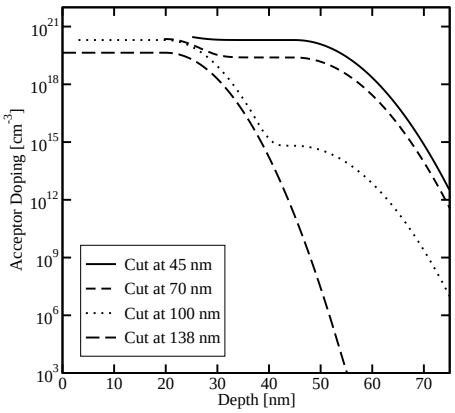


Figure 2: Doping profile displayed on vertical cuts. Depth denotes the vertical distance to the oxide-plane.

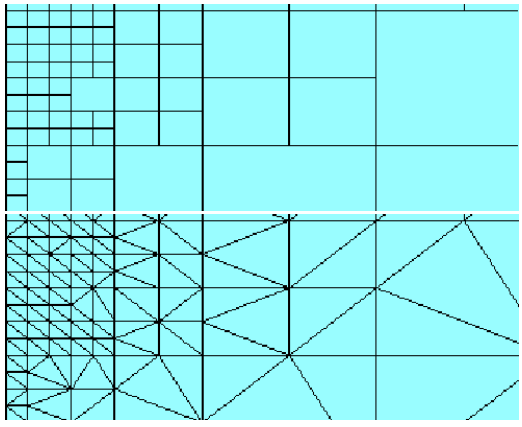


Figure 3: The upper part of the figure shows the recursive quad tree refinement. The corresponding triangularization is shown in the lower part.

carrier concentration as shown in Fig. 5. Proper simulation grids are needed to obtain accurate results with a reasonable number of grid points. This is demonstrated in Fig. 6.

The electric field and the current density of the turned on transistor are shown in Fig. 7 and Fig. 8. The gate capacitance was extracted from a small signal analysis of the device structure (c.f. Fig. 9). It shows the importance of including the spacer and the contact segments. The calculated gate leakage characteristic is given in Fig. 10. The transfer and the output characteristics of the device are shown in Fig. 11 and Fig. 12, respectively.

In conclusion, a quick and accurate TCAD tool which allows to extract the relevant device parameters, based on data which are typically available within a process flow, has been presented.

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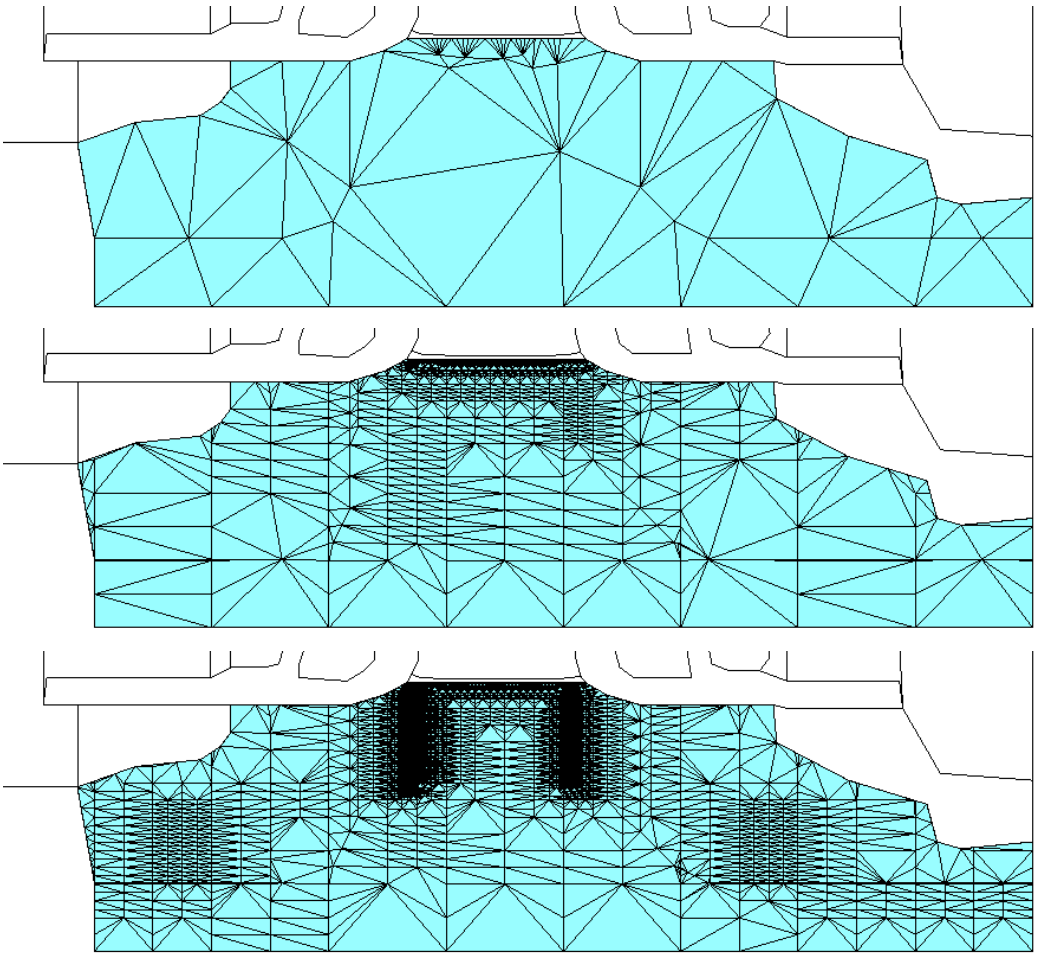

Figure 4: The upper figure shows a minimal triangulation of the geometry. The middle figure shows the channel refinement, and the lower figure the channel and pn-junction refinement.

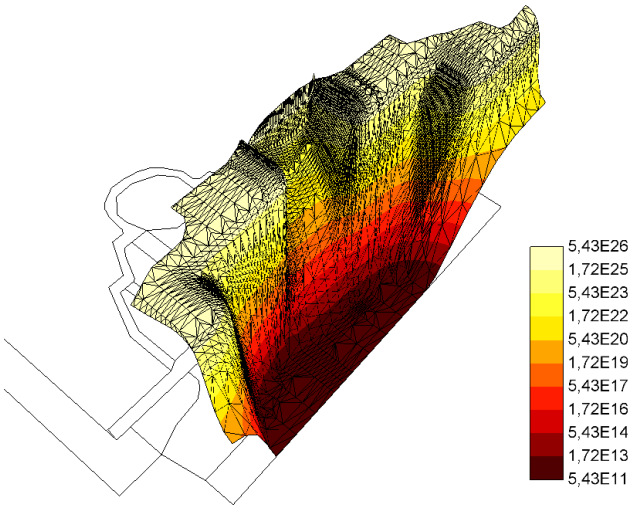

Figure 5: The spatial distribution of the hole concentration in the pMOS transistor ($V_G = -1.5\ V, V_{DS} = -1.5\ V$).

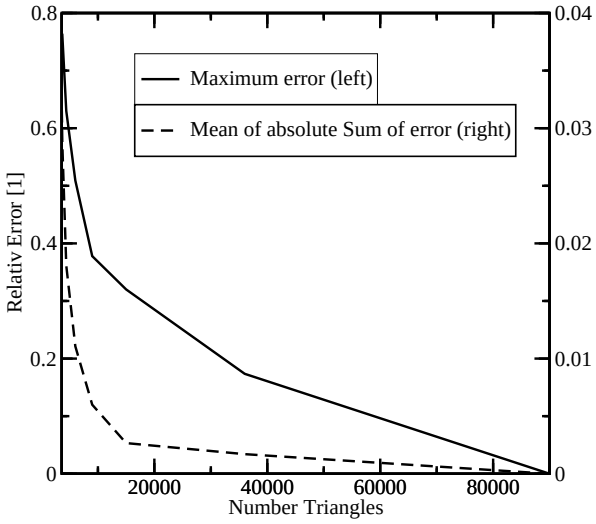

Figure 6: The left and the right axes show the maximum and the mean value of the error in carrier concentration as a function of the number triangles used for the discretization.

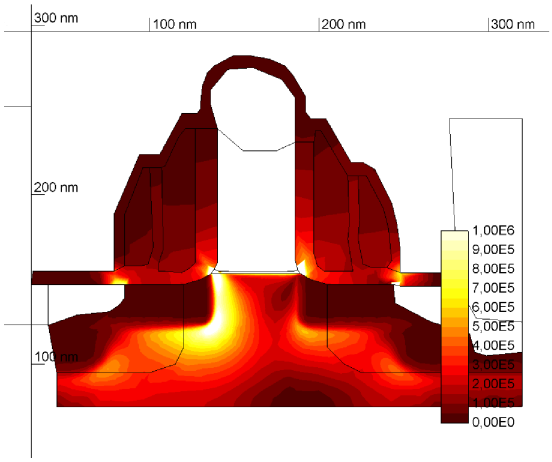

Figure 7: The electric field of the turned on transistor shown at a linear scale.

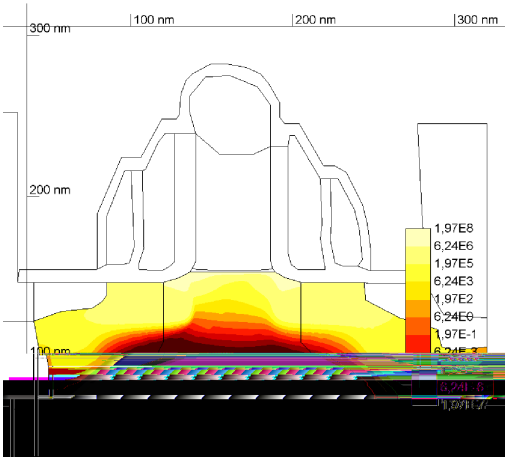

Figure 8: The absolute value of the current density of the turned on transistor shown at logarithmic scale.

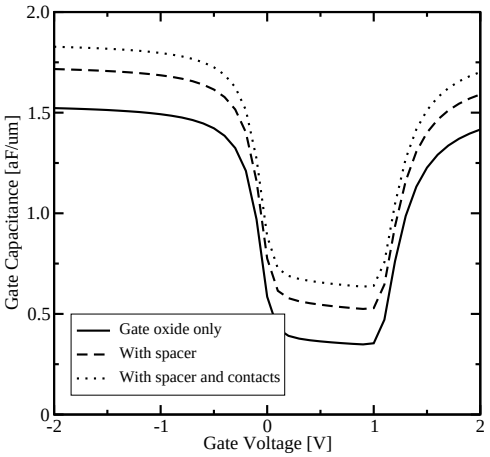

Figure 9: The gate capacitance/voltage characteristic of the structure. Including contacts and spacer to the simulation domain gives rise to an additional coupling.

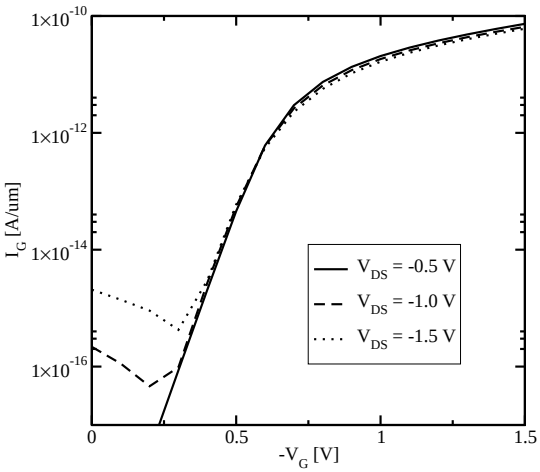

Figure 10: The gate leakage current as a function of the gate bias shown for different drain biases.

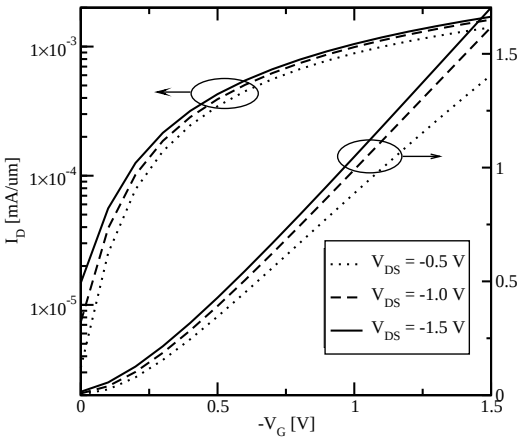

Figure 11: The transfer characteristic of the device on a linear and semi-logarithmic scale.

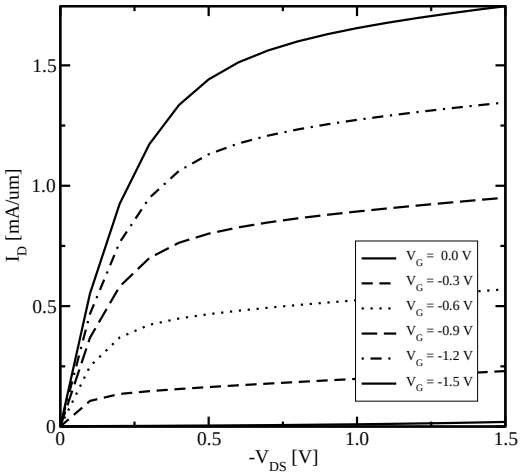

Figure 12: The simulated output characteristics of the pMOS transistor using an energy transport model.

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