Impact of Non-Uniformly Doped and Multilayered Asymmetric Gate Stack Design on Device Characteristics of Surrounding Gate MOSFETs

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ABSTRACT

In the present work, a new structural concept, non-uniformly doped multilayered asymmetric gate stack (ND-MAG) surrounding gate MOSFET has been proposed and it has been demonstrated using analytical modeling and simulation that ND-MAG SGT leads to suppression of short channel and hot carrier effects besides also improving the transport efficiency and gate controllability as compared to UD devices.

Keywords: non-uniformly doped, multilayered asymmetric gate stack, surrounding gate MOSFET, short channel effects, gate controllability

1 INTRODUCTION

The evolution of MOSFET technology has been governed largely by device scaling over the past twenty years. One of the key issues concerning present CMOS design is whether MOSFET devices can be scaled to 0.1μm channel length and beyond for continuing density and performance improvement as continued miniaturization has led to short channel effects (SCEs), hot electron effects and low carrier transport efficiency. In order to overcome the scaling limitations and to enhance the device performance various nonclassical structures such as Pi gate MOSFETs, Omega MOSFET, Cylindrical/Surrounding gate MOSFETs have been proposed. Among these, the surrounding gate MOSFET [1-4], in particular, has drawn a great deal of attention as it offers high packing density, steep subthreshold characteristics and higher current drive. Another remarkable feature of this structure is that the gate surrounds the silicon pillar completely and therefore controls the channel potential in a more effective manner resulting in increased short channel immunity. All these features make the SGT a potential candidate to succeed the classical planar MOSFET.

However, in the nanoscale regime incorporation of alternative device designs is also necessary to improve device performance. In order to address the issues related to short channel degradation and improvement in device performance, the use of non-uniformly doped channel design was suggested as a possible solution for reducing the short channel effects present in deep sub micrometer devices [5-6]. Furthermore, in order to increase the transistor performance, every new technology node requires the reduction of the gate oxide thickness. However, the extent to which gate oxide thickness can be scaled down is limited by direct tunneling. An alternative could be the use of insulator material with a higher permittivity than SiO_2, which would allow a thicker gate insulator. The major advantage of using high-k dielectrics for the gate insulator comes from the fact that while scaling, the significant parameter for constant electric field scaling is not the physical thickness of the gate insulator but rather the capacitance per unit area. However, studies reported that threshold voltage (V_{th}) roll-off, DIBL and subthreshold slope (S) increase with an increase in dielectric permittivity (or thickness) implying that short channel performance degrades [7-8]. This can be attributed to the loss of gate control owing to the increased fringing fields. In order to overcome these detrimental issues, the multilayered asymmetric gate stack oxide design along with the non-uniformly doped design has been incorporated in surrounding gate MOSFET (ND-MAG) SGT. Using modeling and simulation [9], it is demonstrated that ND-MAG provides an effective solution to these drawbacks. It has been demonstrated that incorporation of ND and MAG design leads to an improvement in short channel immunity and hot carrier reliability while also enhancing the gate controllability and carrier transport efficiency and thus ensures better performance as compared to conventional devices. Thus, the critical issues of short channel effects, hot carrier effects and gate leakage can be addressed by incorporating the non-uniformly doped and asymmetric gate stack architectures.

2 MODEL FORMULATION

Fig.1. shows the cross-section view of ND-MAG SGT. As can be seen the channel has two regions, the one near the source is heavily doped and the one near drain is low-doped. Also there is an asymmetric gate stack, i.e., multilayered gate stack is present near the drain and single gate oxide is present near the drain. Thus there is a single gate oxide (SGO) region near the source and a gate stack oxide (GSO) region near the drain.

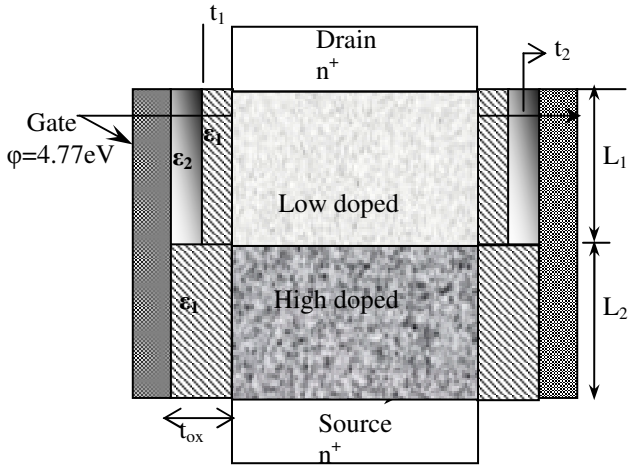

Fig.1. Cross-sectional view of ND-MAG SGT

Assuming the impurity density in the channel to be uniform, the Poisson equation in cylindrical coordinates for the two regions can be written as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_i(r,z)}{\partial r}\right)+\frac{\partial^2 \psi_i(r,z)}{\partial z^2}=\frac{qN_{ai}}{\varepsilon_{si}} \tag{1}$$

where, $\psi_i(r,z)$ is the potential distribution in the silicon film, N_{ai} is the doping concentration with $i=1$ for region 1 near the source and $i=2$ for region 2 near the drain end.

The potential distribution in the silicon film in the two regions is assumed to be a parabolic profile in the radial direction [10] and on solving the Poisson equation in the two regions separately using the boundary conditions [11-12], the surface potential in the two regions is obtained as:

$$\psi_{s1}(z)=A\exp\left(\frac{-z}{\lambda_1}\right)+B\exp\left(\frac{z}{\lambda_1}\right)-\nu_1 \tag{2}$$

$$\psi_{s2}(z)=C\exp\left(\frac{-(z-L_1)}{\lambda_2}\right)+D\exp\left(\frac{(z-L_1)}{\lambda_2}\right)-\nu_2 \tag{3}$$

Where,

$$\nu_1=\frac{qN_{aH}\lambda_1^{\,2}}{\varepsilon_{si}}-\psi_{gs1} \tag{4}$$

$$\nu_2=\frac{qN_{aL}\lambda_2^{\,2}}{\varepsilon_{si}}-\psi_{gs2} \tag{5}$$

where $\psi_{gsi}=V_{gs}-V_{fbi}$ is the gate potential, V_{fbi} is the flatband voltage and ψ_{si} is the potential at the surface of silicon film for regions 1 and 2 respectively and λ_1 and λ_2 are the characteristic lengths given by:

$$\lambda_1=\sqrt{\frac{\eta t_{si}^{\,2}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}{8}} \tag{6}$$

$$\lambda_2=\sqrt{\frac{\eta t_{si}^{\,2}\ln\left(1+\frac{2t_{oxeff}}{t_{si}}\right)}{8}} \tag{7}$$

where, $\eta=\varepsilon_{Si}/\varepsilon_{ox}$, t_{si} is the thickness of silicon film, t_{ox} is the oxide layer thickness of SGO region and t_{oxeff} is the effective oxide layer thickness of the GSO region in terms of the corresponding thickness of the SiO_2 layer and is defined as:

$$t_{oxeff}=t_1+\frac{\varepsilon_1}{\varepsilon_2}t_2 \tag{8}$$

where, t_1 is the thickness of the SiO_2 layer and t_2 is the thickness of the high-k layer. The coefficients A, B, C and D have been obtained using the conditions of continuity for potential and electric field at the interface of high and low doped regions.

The position of minimum surface potential, z_{min} is calculated by differentiating (2) w.r.t. z and equating the resulting expression to zero.

$$z_{\min}=\frac{\lambda_1}{2}\ln\left(\frac{A}{B}\right) \tag{9}$$

The minimum surface potential is then obtained from (4) as:

$$\psi_{s1\min}=2\sqrt{AB}-\nu_1 \tag{10}$$

The electric field distribution in the high and low doped region can be obtained by differentiating $\psi_{s1(z)}$ and $\psi_{s2(z)}$ respectively.

The threshold voltage, V_{th} can be obtained by equating the minimum surface potential ψ_{s1min} to $2\psi_{f1}$ and the expression for threshold voltage is obtained as:

$$V_{th}=\frac{-b+\sqrt{b^2-4ac}}{2a} \tag{11}$$

where, a, b and c are the various coefficients obtained in the analysis.

Subthreshold slope, S, is defined as:

$$S=\frac{kT}{q}\ln(10)\frac{1}{\frac{\partial \phi_s(z_{\min})}{\partial V_{gs}}} \tag{12}$$

Thus, S can be obtained by using (10) in (12).

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3 RESULTS AND DISCUSSION

Fig.2 shows the variation of surface potential and electric field with channel length. It is seen that ND-MAG exhibits a step function in the surface potential profile as compared to UD device which screens the region near the source from variations in drain voltage and hence ensures more reduction in DIBL. Moreover, average electric field under the gate is higher for ND-MAG which improves the carrier transport efficiency. The peak electric field near drain is lower implying reduction in impact ionization.

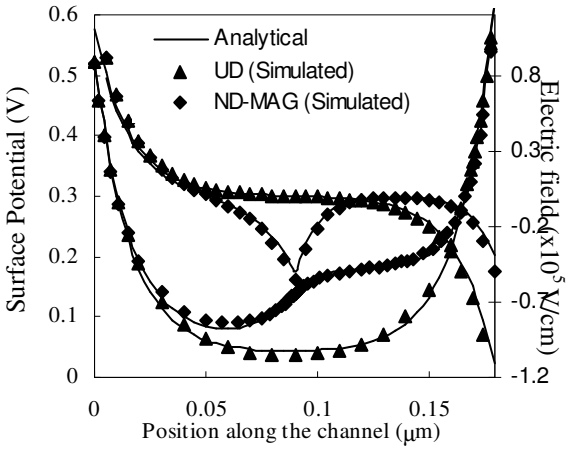

Fig.2. Variation of surface potential and electric field along the channel for L=180nm, L_1=90nm, t_{ox}=5nm, t_{Si}=75nm, $N_H=3x10^{23}m^{-3}$, $N_L=6x10^{22}m^{-3}$, t_1=1nm, t_2=4nm, ε_2=20, V_{gs}=0.2V, V_{ds}=0.1V.

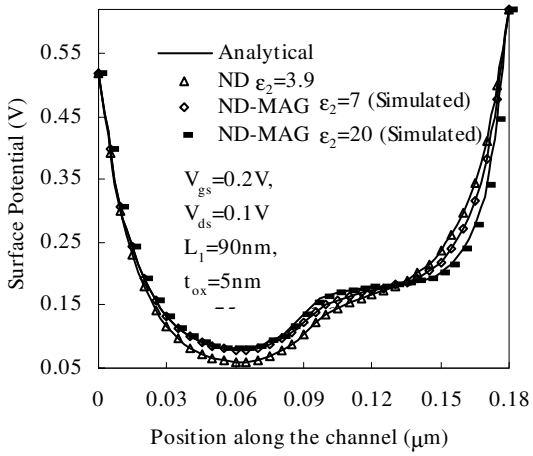

Fig.3 Variation of surface potential along channel for different values of the dielectric constant of the upper dielectric layer, ε_2

Fig.3 shows that as ε_2 increases, the minimum surface potential decreases implying a better gate controllability and therefore increased short channel immunity. Fig.4 shows that V_{th} roll-off is considerably reduced by incorporating ND-MAG design. Fig.5 shows the variation of DIBL with channel length and it is seen that DIBL is lowest for ND-MAG as compared to UD devices.

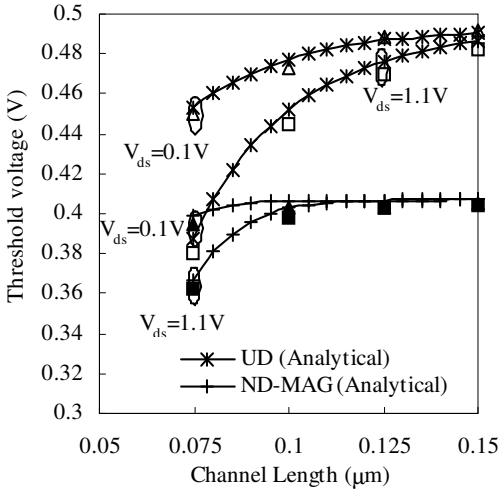

Fig.4 Variation of threshold voltage with channel length.

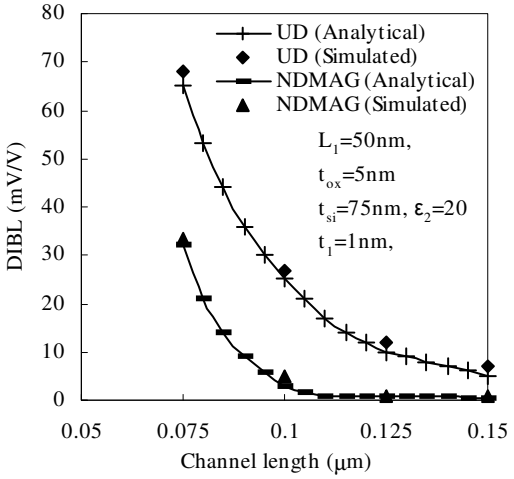

Fig.5 DIBL variation with channel length for UDand ND-MAG devices.

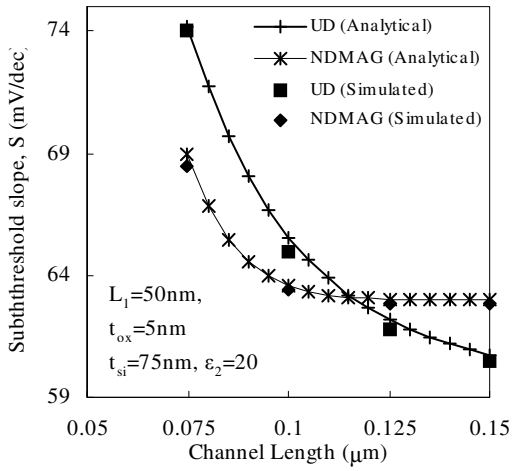

Fig.6 Variation of subthreshold slope with channel length.

In fig.6, the analytical and simulated results showing the variation of subthreshold slope with channel length has been plotted for the devices. It is found that on increasing the dielectric constant of the upper dielectric layer, ε_2 of the gate stack region, that is, on introducing MAG design, the subthreshold slope reduces considerably which again confirms that short channel immunity can be improved by incorporating MAG design.

4 CONCLUSION

A two-dimensional analytical model for a new structural concept ND-MAG (non-uniformly doped multilayered asymmetric gate stack) SGT has been developed and its impact on the device characteristics has been analyzed. The analytical results so obtained have been compared with the simulated results obtained from the device simulator ATLAS and have been found to be in good agreement. It has been demonstrated that the magnitude of the positive offset voltage is higher for ND-MAG as compared to UD devices which ensures better screening from drain bias variations leading to a reduction in DIBL. The effectiveness of ND-MAG design can also be seen as a reduction in V_{th} roll-off and subthreshold slope. Moreover, the peak in the electric field distribution under the gate is higher for ND-MAG as compared to UD devices, which ensures uniformity in the average drift velocity of the electrons in the channel which results in an improvement in the carrier transport efficiency. In addition, ND-MAG design also leads to a reduction in the peak electric field near the drain end as compared to UD devices which implies a reduction in hot carrier effects. The study thus affirms the fact that incorporation of ND and MAG designs ensures better performance as compared to UD devices.

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