Modeling of gain in advanced CMOS technologies

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ABSTRACT

The impressive downscaling of CMOS technology and its more and more massive introduction in System-on-Chip (SoC) oriented applications require a modeling approach able to describe new physical effects paying attention to such different environments (digital and analog) coexisting in a single technological platform for SoC. In particular, in this paper we deep insight the modeling of gain, a key parameter ruling the analog performances in relation with their layout dependence affected by the shallow trench isolation (STI) induced mechanical stress. Both n- and p-channel have been investigated as a function of temperature. The W scaling modeling has been dealt with for the first time. A 90 nm CMOS advanced technology for Embedded Flash applications has been characterized.

Keywords: gain, compact modeling, mobility, temperature, *W* scaling

1 MODELING OF GAIN

The gain parameter of MOSFET plays a crucial role in analog design. It is so defined in linear region:

$$g_m = \mu_0 \cdot \frac{\varepsilon_{OX}}{t_{OX}} \cdot \frac{W - \Delta W}{L - \Delta L} \cdot V_{DS} \qquad (1)$$

where μ_0 is the low-field mobility, ε_{ox} the relative oxide dielectric constant, t_{ox} the electrical oxide thickness, W and L the MOSFET channel width and length, ΔW and ΔL the width and length variations, respectively. V_{DS} is the drain-source bias. The accurate definition of transconductance becomes related with the capability to well describe μ_0, that is modulated by temperature and geometrical features (modulating the mechanical stress) and doping, being other terms, in principle, constant. However, in ultra-scaled CMOS technologies, it is not a trivial problem to discriminate the correlations between ΔW, ΔL terms and μ_0. A 90 nm CMOS technology for Embedded Flash applications has been characterized.
This work starts dealing with the correct characterization and modeling of the channel geometrical definition (ΔW and ΔL), then the low-field mobility dependence as a function of temperature, layout, type of channel doping. A novel modeling trend on the gain versus W is tackled. Conclusions follow.

1.1 ΔL and ΔW extraction

Let's start to consider the extraction of ΔL and ΔW parameters. The well known low-field mobility modification as a function of SA layout parameter has been recently introduced in BSIM 4 compact model [1].

Fig. 1 shows the ΔL values obtained from the typical extraction plot reporting $1/g_m$ vs. L as a function of different SA parameters (see inset of Fig. 1)..

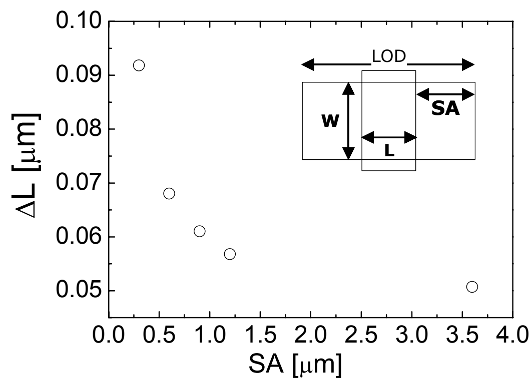

Fig. 1: Extracted ΔL parameters vs different SA parameters with the 'classical' method.

Different ΔL values are obtained for various SA bringing into question the real value of a so obtained ΔL. Recently a new methodology to extract the layout value based on the capacitance measure was proposed [2]. To avoid the complication related with that approach (i.e. the parasitic capacitance determination and the bias dependence), we propose the simpler method of the linear regression of the inverse of gain vs L scaling, but using STI-stress free test structure of Fig. 2 annihilating the effect of strain on the low-field mobility. Fig. 3 shows the good comparison of results obtained by using the proposed strategy and the C-V method. This result has been also validated by means of the comparison with device TCAD simulations through which we have estimated ΔL when the I-V experimental curve of the short channel MOSFET was reproduced via numerical simulation after the low-field mobility calibration in the long-channel device.

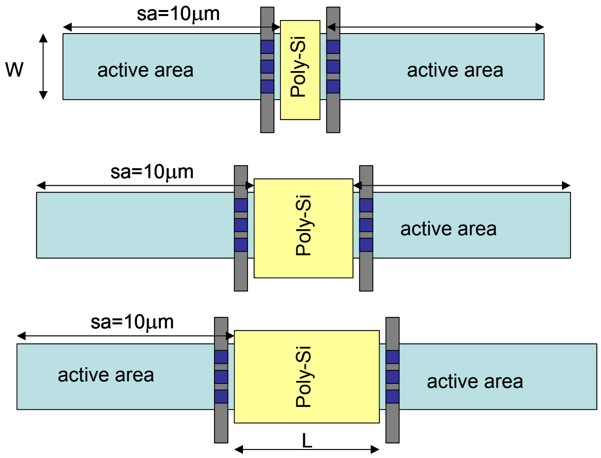

Fig. 2: Layout of the proposed STI-stress free.

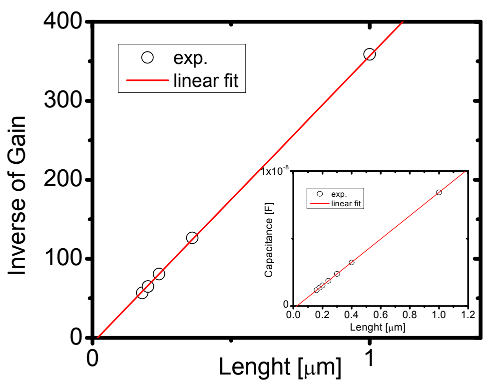

Fig. 3: Extracted ΔL parameters from both STI-stress free structures and C-V method.

1.2 Low field mobility: temperature

Let's move to consider the low-field mobility (μ_0). It is well-known that it strongly depends on temperature (Fig. 4) reports the mobility trend in the usual temperature operative range of different families of devices showing that, as rule of thumb: $\mu_0(T) \propto T^{-3/2}$ for the *n*-channel and $\mu_0(T) \propto T^{-1}$ for *p*-channel. These trends are coherent with the more pronounced phonon scattering dependence for electrons and coulombic scattering for holes. In fact, holes, being slower than electrons, are more affected by the Rutherford scattering with ion impurities [3]. This experimental finding is to be taken into account when delay chain containing both *n*- and *p*-channel MOSFETs must be calibrated as a function of temperature. A more linear trend of holes versus temperature in comparison with electrons can also be observed considering *p*-well against *n*-well resistors [4].

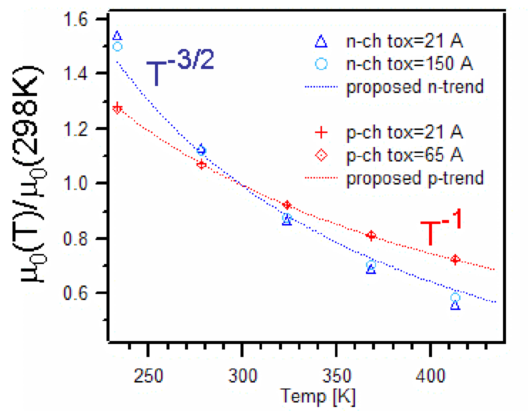

Fig. 4: Normalized temperature trend of low-field mobility for both *n*- and *p*-channel showing unchanged trend considering different technologies

1.3 Low field mobility: Mechanical stress effects

Then, STI-induced mechanical stress affects the low-field mobility of both electrons and holes as a consequence of the strain-altered band structure [5]. As it concerns the conduction band modification we take for granted the deformation-potential theory defining a rigid shift of its bottom edge produced by a homogeneous strain [6]. In particular, the energy shift of the six conduction band valleys induced by the presence of stress can be written as a linear combination of the strain tensor components and the deformation potential constants:

$$\delta E_{nk} = \sum_{j=1}^{6} \Xi_j \cdot u_j \qquad (2)$$

where δE_{nk} is the shift of the energy at the band edge point k due to a strain with components u_j referred to the crystallographic axes. In summary, the effect of strain can be reviewed as a rigid energetic shift without altering, in the framework of this theory, the dispersion shape of the conduction band (CB). This shift causes the conduction band repopulation and so, in terms of MOSFET performance, a change in low-field mobility. In fact, this will generate a size modulation of ellopsoidal isoenergy surface corresponding to the CB minimum closed to X position of the Brillouin zone and, consequently, an effective mass change that will vary the device transport properties. Using a classical approach (Boltzmann distribution: $n_{0nk}=N_c \cdot e^{-(E_{0nk}-E_F)/kT}$) the fractional change in

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electron density for each valley with δE_{nk} energetic shift is given by:

$$\frac{\delta n_{nk}}{n_{0nk}} = -\frac{1}{kT} \cdot \delta E_{nk} \qquad (3)$$

where δE_{nk} is calculated from (2).

Indeed, there are two factors leading to the increased mobility: reduced effective mass and reduced intervalley scattering. Scattering is reduced because low energy electrons only access to iso-energy valleys.

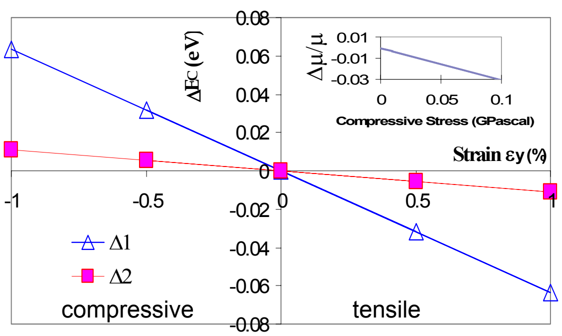

Fig. 5: Shift of the conduction band edge under a uniaxial stress applied along the W direction for the 4 valleys (Δ1) of the (001) plane and for the Δ2 valleys. Inset: the related mobility reduction.

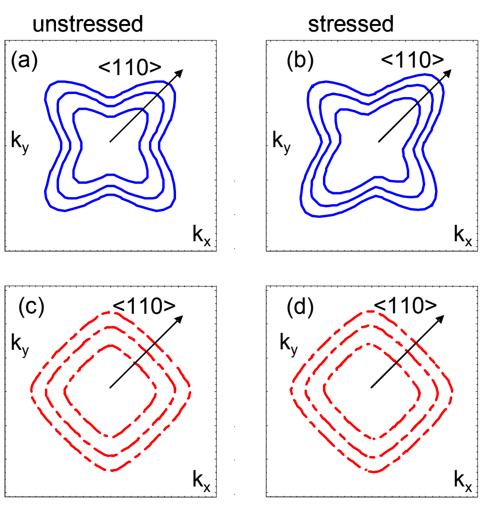

Fig. 6: a) Relaxed Silicon: isoenergy surface plot of the Heavy Holes (HH) at 10,20,30 meV with respect to the top of the valence band b) Compression of 1 Gpascal along the W direction; the band structure of HH are shifted and modified, reducing the mobility. c) Light Holes band, relaxed silicon; d) Same compression of b) for LH

Therefore, we can study the impact of stress constrain in *n*-MOS device as a consequence of the minimum conduction band energy shift induced by the mechanical stress presence. Fig 5 reports the so determined energetic shift for the conduction band. Values of Ξ_j can be deduced from ref. 6 and, in the inset, the related mobility variation.

For the valence band, we choose to describe the Bir-Pikus theory considering both the degeneracy lift between light and heavy holes and the bands dispersion deformation [7]. In Fig. 6a) and 6c) the constant energy surface of both heavy holes (HH) and light holes (LH) for relaxed silicon is pictured. The "matrix element" parameters for the valence band computation have been captured from literature [2] together with the deformation-potential values [3]. In fig. 6b) and 6d) the light and heavy holes band energy dispersion in the $\boldsymbol{k}_x$, $\boldsymbol{k}_y$ conduction plane has been plotted for the strained silicon under a compression in the *W* direction of 1 GPascal. As previously noted [9], in the case of the conduction band the stress-induced enhancement of the subbands shift cannot explain the mobility modification. We note that for uni-axial compression the increased occupation along the [-110] direction (where the density of states is higher) leads to decreased the transport effective mass for conduction in the [110] direction because of the steeper gradient of the band structure in this direction, and consequently a decreased mobility and drive current.

Fig 7 reports the so determined energetic shift the strain-altered valence band in the [110] channel direction.

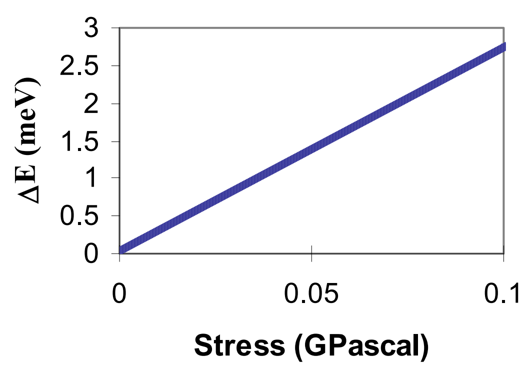

Fig. 7: Energetical separation between the top of the HH and the LH bands under a uniaxial stress applied along the *W*. The hole mobility reduction cannot be explained only by this phenomena

1.4 Transconductance trend vs *W*

Figs 8 and 9 show a non monotonic trend of the *W* normalized gain as a function of *W* for both *n*-channel and *p*-channel, respectively.

The initial gain lowering with W scaling up to around 1 µm can be ascribed to the low-field mobility decreasing by the lateral STI-induced stress coherently with the altered band structure shown in Figs. 5, 6. This behavior can be taken into account with the introduction of a monotonic μ_0 dependence vs *W* for both electrons and holes (dashed lines in Figs 8 and 9).

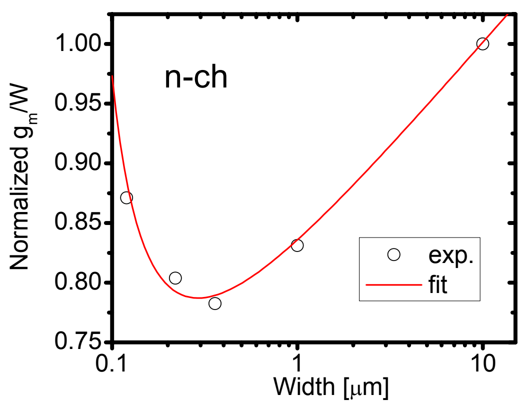

Fig. 8: *n*-channel normalized ratio of g_m/W as a function of *W* showing two regimes: decreasing for STI stress and increasing for ΔW. A good match with the proposed dependence.

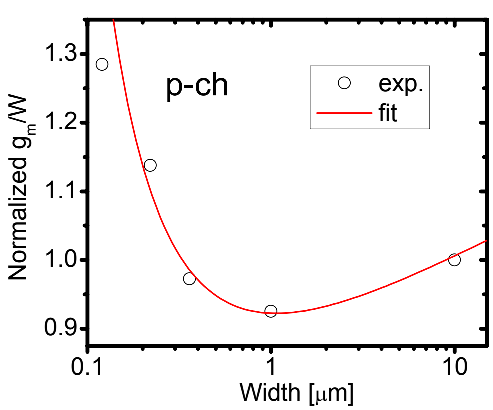

Fig. 9: *p*-channel normalized ratio of g_m/W as a function of *W* showing two regimes: decreasing for STI stress and increasing for ΔW. A good match with the proposed dependence.

The non-monotonic experimentally observed can reproduced, with the ΔW introduction that plays an opposite role (enhancing the gain) for the narrower structures. This also correlates with ID_{SAT} trend just observed in [10]. Then, we suggest to improve the low-field mobility expression with the introduction of *W* dependence in standard compact models. Finally, in a standard parameters flow extraction we suggest to fit this gain behavior to compute the value of ΔW. On the contrary, it is important to avoid obtaining the ΔW value from the gain scaling versus *W*, since STI mechanical stress gets dirty the extraction.

2 CONCLUSIONS

Summarizing, we investigated the modeling of gain in advanced CMOS technologies. We addressed a new methodology to pay an accurate attention to the layout dependence, due to the role of STI mechanical stress, in the 'classical' ΔL determination. With the support of both strain-altered band structure modeling and experimental data, a new expression for the low-field mobility dependence on *W* has been proposed. The method should push a strong improvement in the next generation mixed-signal design.

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