

Adaptable Simulator-independent HiSIM2.4 Extractor

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ABSTRACT

This paper presents a method and its software implementation to extract Spice parameters of the HiSIM2.4 (Hiroshima-university STARC IGFET Model) surface-potential-based model [1, 3]. The completed flow of dedicated parameter extraction procedures is currently designed for the HiSIM2.4 model and can be a potential base to cover the upcoming HiSIM-LDMOS model which was recently selected by the CMC as a new standard for High Voltage MOSFET devices. A unique feature of this approach is that the underlying measured data base is collected independently and can be accessed to generate any standard MOSFET model. Other models like PSP, BSIM3/4 or EKV3 [10] can be generated within the same framework from the common measurement database [4-9]. The parameter extraction routines are based on highly efficient direct extractions, taking into account all HiSIM2.4 modeled effects important for advanced CMOS devices with extremely reduced device feature sizes in the process nodes 65/45nm and beyond. Moreover, the set of local optimizations and interactive tuners is available for all standard IV, CV curves and S-par characteristics as well as special PCM like diagrams to guaranty a high level of the simulation model scalability. Besides the basic DC and CV parameters, high frequency effects are taken into account to enable the usage of the simulation model in analog/RF designs as well. The presented software package is competed with a reporting module for effective results analysis using graphs and data visualization. Furthermore, the procedures are highly automated to assure the accuracy and quality of released Spice-level models.

Keywords: parameter extraction, compact modeling, PSP, HiSIM, EKV, LDMOS

1 INTRODUCTION

Simulations of advanced CMOS circuits, in particular, for analog/RF applications require technology specific libraries with Spice model parameters. Existing typical procedures determine parameters in sequence and neglect the interactions between target parameters and, as a result, the fit of the model to measured data may be less than optimum. Moreover, the parameters are extracted in relation to a specific device and, consequently, they

correspond to different device sizes. The extraction procedures are also generally specific to a particular model, and considerable work is required to change or improve these models.

This paper describes the application of a general-purpose method and its software implementation allowing to obtain a complete set of parameters for any arbitrary model. This extraction method is implemented in the IC-CAP, measurement and parameter extraction software. The HiSIM 2.4 model has been selected to illustrate the method and its flow. After a brief review of the HiSIM 2.4 model, section 2 discusses the measurement data base architecture, section 3 outlines the HiSIM specific extraction flow and presents the results obtained by the proposed extraction method. Section 4 summarizes the conclusions derived in this investigation.

1.1 HiSIM 2.4 Model

HiSIM (Hiroshima-university STARC IGFET Model) is a surface-potential-based MOSFET model developed by Hiroshima University and the STARC organization [1, 3]. Using the charge sheet approximation and the gradual-channel approximation, all device characteristics are described analytically by channel-surface potentials at the source side and at the drain side. The surface potentials are obtained by solving the Poisson equation with the Gauss law using an iterative algorithm. The HiSIM model solves the Poisson equation iteratively without introducing any assumptions, similar to the 2-D numerical simulator and accurately yields the resulting characteristics. All phenomena such as advanced mobility model, short-channel and reverse-short-channel effects are included in the surface potential calculations. The advanced technologies accompanied by aggressive downscaling of device sizes cause various phenomena such as short-channel effects, namely: short-channel and reverse short-channel effect are consisting in the HiSIM 2.4 model. All the observed short channel effects are caused by lateral electric field contributions in the MOSFET channel. The reverse short-channel effect, mainly associated with the pocket implant technology, causes the nonuniform impurity concentration along the channel. The model parameters describing the extension of the pocket are included in HiSIM. Therefore, an important advantage of the HiSIM 2.4 modeling approach is that detailed information about the fabrication technology allows to precisely characterize

device variations. Moreover, the short-channel and reverse short-channel effects are integrated as the threshold voltage shift together with polydepletion and narrow width effects. The HiSIM model also preserves technology independent mobility universality conditions with the low field mobility described by three independent mechanisms of coulomb, phonon, and surface roughness scattering.

1.2 HiSIM LDMOS Extension

The HiSIM-LDMOS model preserves all the features of the bulk-MOSFET HiSIM model with extensions specific to the modeling of the drift region [2, 11]. The potential distribution along the LDMOS extension region is described by solving the Poisson equation iteratively, including the resistance effect of the drift region. LDMOS self-heating effect simulations are possible by applying an internal thermal network.

2 DATABASE ARCHITECTURE

A unified environment was developed to enable the generation of several MOS model types based on a common data base of measured data. The basic idea of this concept is described in [9].

2.1 Advanced data representation

To enable an effective parameter extraction it is critical to prepare the measured device data in such a way that a certain effect, e.g. an effect related to channel length or a temperature effect, can be clearly identified in the data set. However, typically the classical MOS related curves (e.g. i_d vs. v_g or i_d vs. v_d) are measured from a huge amount of devices. Therefore, it is necessary to generate the above mentioned data sets with special data base operations [4-9]. An example of such curves can be seen in the Fig. 1 and 2.

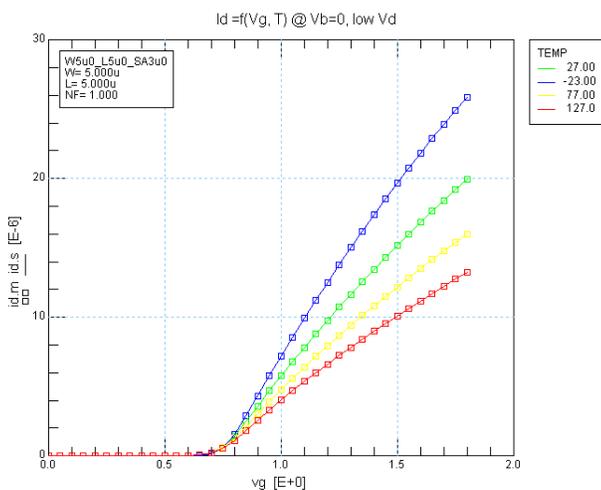


Figure 1: The i_d vs. v_g plots at different temperatures

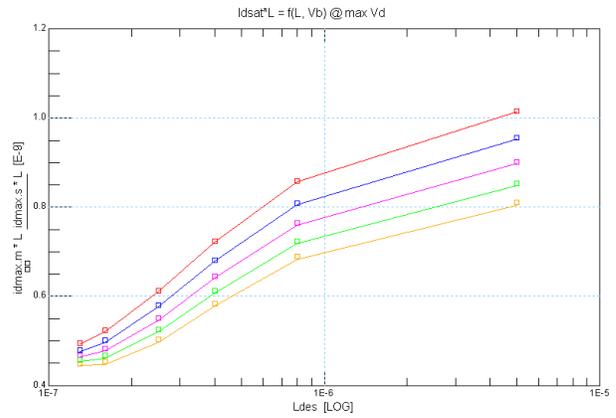


Figure 2: On current I_{on} at different gate lengths

2.2 Data Flow

The following sketch in Figure 3 shows the principal data base operations which are necessary to generate the i_d vs. v_g diagram at different temperatures, given in Figure 1. First, we have a collection of i_d - v_g and i_d - v_d curves for different devices at different temperatures. This is the set of raw data typically measured in the lab. We put all this data into a database and can now derive subsets of the data with a reduced amount of operating conditions (v_g , v_d , etc.) over a range of temperatures and devices geometries.

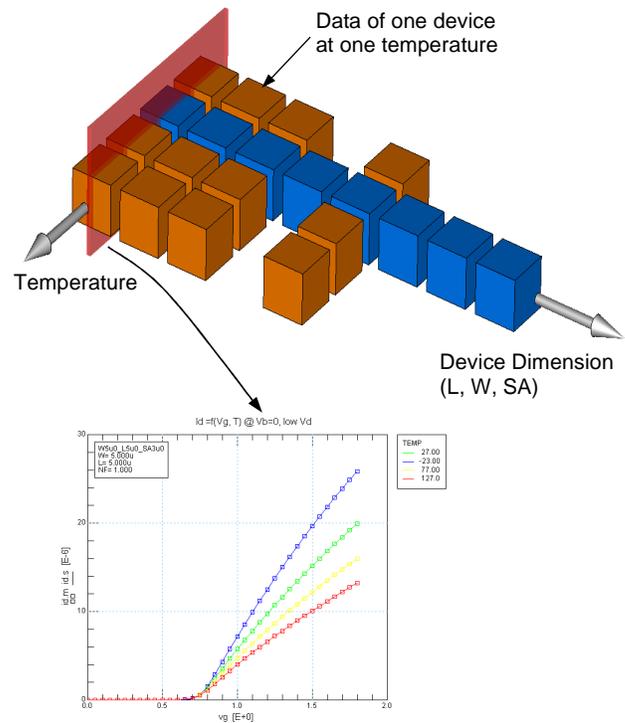


Figure 3: Data base operation to derive an i_d vs. v_g diagram at different temperatures

3 HISIM 2.4 SPECIFIC EXTRACTIONS

3.1 Requirements for Parameter Extractions

The complexity of state of the art CMOS processes requires a very dedicated strategy in extracting model parameters. Due to the large diversity of process flavors e.g. having low threshold voltage (V_{th}), high V_{th} and native V_{th} devices, the amount of simulation models to cover those flavors is steadily increasing. Therefore, the requirements for an effective model parameter extraction program are the following:

- Extractions should be adoptable to different process generations from a minimum feature size of 0.18 μ m down to 32nm
- Extraction functions for certain parameters should be intelligent in such a way that they can identify reasonable regions from given curves (like i_d vs. v_g at low v_d) to extract the desired parameters
- The complete extraction procedure should be repeatable and should not depend on the operator.
- Finally, it should be possible to automate the extraction process to enhance productivity in the modeling groups.

We will discuss these requirements in the following sub chapters and show how we solved those issues.

3.2 Special Emphasis on Scalability and Analog Behavior

It is desirable for selected applications (digital, analog/mixed-mode, RF and high voltage) to apply only one set of model parameters for each of the currently used transistors (i.e. the n- and p-channel MOS devices) because circuit simulations can then be performed by only specifying the type and dimensions of the transistors.

The MOS model extraction procedures include steps of the DC and AC parameterization to extract the final model. Model extraction flow is divided into geometrical (in the entire range of L's and W's) and bias regions (sub-threshold, linear and saturation) for different device types applying recommended DC/AC sweeps. The sweeps could be application-specific for CMOS processes targeting digital applications only (i.e. drain current, intrinsic capacitances, leakage); analog/mixed-mode technologies (transconductances and output conductances G_m/G_{ds} , higher order derivatives, etc.); RF (maximum operating frequencies, noise performance, etc.); and high voltage (I_{ds}/V_{dsmax} , I_{ds}/V_{gsmax} at operation bias conditions).

Finally, both DC and AC characteristics of the extracted model for the available W/L geometry range is used to extract and verify device temperature scaling at least at three different temperatures (e.g., -40°C, 27°C and 125°C for automotive applications) and subsequently repeated for the linear and saturation operation regions.

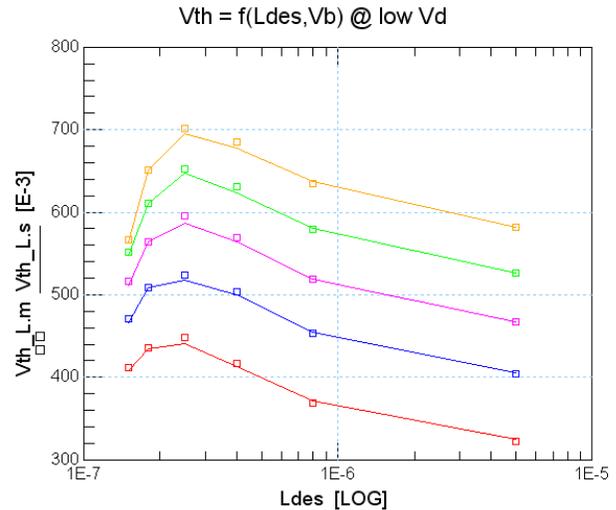


Figure 4: Example of $V_{th}(L)$ scaling

Extraction of the extrinsic model parameters (i.e. junction and overlap capacitances) or specific RF model extensions are an integral part of the extractor and are available as dedicated modules.

3.3 Direct Extractions, Optimization and Tuner Routines

As the HiSIM device characteristics are strongly dependent on basic device parameter values (i.e. gate dielectric parameters, coefficient of gate length and width modification) it is recommended to start with initial parameter values (not changing during extraction procedure) according to the reference documentation [1, 3].

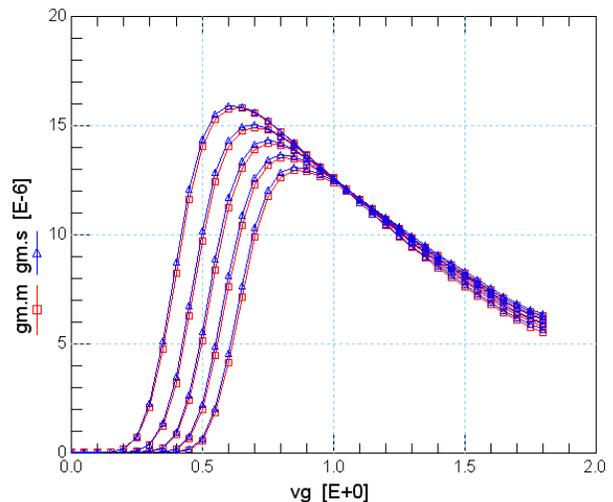


Figure 5: The g_m curves used for mobility modeling

Basically, the most important extraction of the HiSIM surface potential-based model are its intrinsic device parameters such as gate oxide thickness (TOX) as well as channel and substrate doping concentrations (NSUBC,

NSUBP), since they mostly determine the device features [3]. Within the extraction package, these parameters can be extracted from measured data or can be set as initial values, if information about device parameters is available before starting extraction. The first step of IV extractions is VFBC and NSUBC parameter determination using back bias dependent Id-Vgs data of the large (long-wide channel) device. VFBC is directly extracted using the relation

3) models the Vth decrease with Lgate decrease. These parameters are tuned to fit the measured Vth-Lgate characteristic. Note that SCP2 and SC2 are modeling Vds dependency of the SCE, so other Vds related parameters, such as high-field mobility and channel-length modulation (CLM), are to be tuned together with those two parameters. The main extraction sequence is briefly summarized in Table 1 for the core IV measurements.

Table 1: Main HiSIM Extraction Sequence

Step	Target Data	Extractions
(a) rough extraction around Vth or lower		
1	Large IdVg	VFBC, NSUBC
2	L_Scale IdVg	LP, NSUBP
3		SCP1, (SCP2), SCP3
4		SC1, (SC2), SC3
		PARL2
(b) rough extraction around Vth or higher		
5	Large IdVg	MUECB0, MUECB1
		MUEPH1, MUESR1
6	L_Scale IdVg	XLD
7	W_Scale IdVg	XWD
(c) rough extraction with IdVd in the lin & sat regions		
8	Short IdVd, IdVg	XLD, RS, (RD)
9	Short IdVd	VMAX
		VOVER, VOVERP
10		CLM1, CLM2, CLM3
		CLM5, CLM6
11	Large IdVd	MUEPH1, MUESR1
(d) rough extraction around Vth or higher		
12	Short IdVg	MUEPHL, MUEPLP
		MUESRL, MUESLP
13	W_Scale IdVg	WFC, WVTH0
14	Narrow IdVg	MUEPHW, MUEPWP
		MUESRW, MUESWP
(e) fine extraction with IdVg in the subthreshold regions		
(f) fine extraction with IdVd in the lin & sat regions		

between threshold and flat-band voltage taking the surface potential effect into account. These two parameters basically model the Vbs-dependent drain current of the large device, especially around threshold voltage or at lower Vgs. The mobility model has an impact on the current behavior in the region of Vgs above threshold voltage, where current flows through the channel. Within the extraction package, mobility parameters are initially extracted using the calculated effective mobility curve based on measured data (Fig.5). After initial extraction, these mobility parameters are optimized to fit Id and its derivatives versus Vgs characteristics. For short-channel effect (SCE), LP plays an important role to model the Vth-Lgate characteristic. LP is extracted from measured Lgate dependency of Vth data. LP and NSUBP together with SCPn (n=1 to 3) are modeling the Vth increase with Lgate decrease caused by pocket implant technology. SCn (n=1 to

4 CONCLUSION

In this paper, a new method and its software implementation has been presented to extract parameters of a compact MOSFET model. In our case, dedicated direct extraction routines as well as optimization and parameter tuning steps have been applied. The approach can be easily generalized to extract multiple features at all available characteristics based on measurement data. The interactive extraction flow can be automated, allowing user independent processes to enhance the productivity.

Although the HiSIM 2.4 model was used to demonstrate the results, any other compact model, i.e. the HiSIM-LDMOS model can be easily implemented in a similar fashion.

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