Improved Carrier Mobility in Compact Model of Independent Double Gate MOSFET

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ABSTRACT

We have already developed an explicit threshold voltage based compact model of independent double gate (IDG) MOSFET which works well for gate length between 30 nm and 1µm, or more [1]. However, the mobility was assumed constant. In this paper, a model with adapted carrier mobility degradation due to the transverse electrical field and velocity saturation is presented.

Keywords: compact model, mobility degradation, velocity saturation, independent double gate MOSFET.

1 INTRODUCTION

IDG MOSFET is a particularly promising device, which is expected for sub-32nm node. To take advantage of the second gate, which can be driven independently and to create new circuits, a compact model including mobility degradation and saturation velocity is essential.

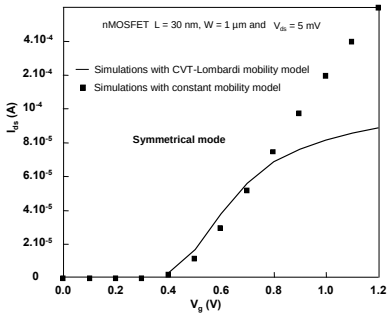

Figure 1: comparison of the drain current with and without a mobility degradation model.

Indeed, Fig. 1 shows a comparison of the drain current versus the gate voltage in symmetrical mode with constant and degradation mobility models. The difference at high transverse electrical field is very important. That is why a mobility model which takes into account the impact of the transverse fields is necessary. Same conclusion is drawn at high lateral field. Identical phenomenon is observed when gates are independently driven.

Consequently, an explicit 2D compact model of IDG MOSFET with an adapted mobility model is developed. The model is a threshold-voltage (V_{th}) based compact model. Firstly, the threshold-voltage based compact model is briefly quoted. Then, we show how mobility degradation and saturation velocity are added in the core of the model. Finally, the model is confronted to Atlas numerical simulations [2] to show and prove its accuracy.

2 EXPLICIT V_{TH} MODEL

Fig. 2 shows the IDG MOSFET structure. L is the gate length, T_{si} is the silicon film (or body) thickness, T_{ox1} and T_{ox2} are the front and the back gate oxide thicknesses. V_{g1} and V_{g2} are the front and the back gate voltages, respectively. $\Delta\Phi_{m1}$ and $\Delta\Phi_{m2}$, which are the work function differences between the front (respectively back) gate and the intrinsic silicon are supposed zero. The silicon film is supposed undoped.

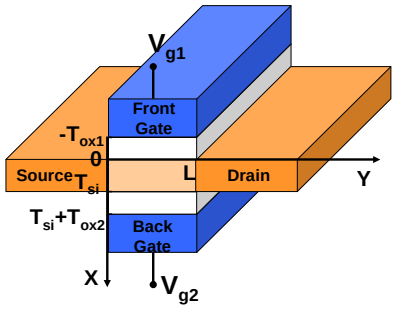

Figure 2: IDG MOSFET.

We begin with the core of the IDG compact model developed in recent years [1,3]. It is a totally explicit threshold voltage based model written in Verilog-A language. Moreover, this model is continuous from weak to strong inversion and from linear to saturation regime. It also takes into account physical short channel effects in the case of independently driven gates. Finally, this model also addressed the case of symmetrical devices when $V_{g1}=V_{g2}$, $T_{ox1}=T_{ox2}$ and $\Delta\Phi_{m1}=\Delta\Phi_{m2}$ and asymmetrical ones when $T_{ox1}\neq T_{ox2}$ and/or $\Delta\Phi_{m1}\neq\Delta\Phi_{m2}$.

3 ADAPTED CARRIER MOBILITY MODEL INCLUDING VELOCITY SATURATION

3.1 Empirical model

We start with the Lombardi mobility model [4], the same used in the ATLAS numerical simulations [2]. This model includes optical intervalley and acoustic phonons, surface roughness and velocity saturation. Optical and acoustic phonons decrease the mobility for a middle transverse electrical field $E_\perp$ whereas the surface roughness acts at high field.
The model starts from the Matthiessen rule:

$$\frac{1}{\mu} = \frac{1}{\mu_{AC}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} \tag{1}$$

where μ_{AC} accounts for the acoustic phonons, μ_b for the bulk mobility and μ_{sr} for the surface roughness.
The mobility due to the transverse electrical is empirically described as:

$$\frac{1}{\mu} = \frac{1}{\frac{4.75\times10^{7}}{E_\perp} + \frac{1.5\times10^{4}}{E_\perp^{1/3}}} + \frac{1}{1417} + \frac{1}{\frac{5.82\times10^{14}}{E_\perp^{2}}} \tag{2}$$

These parameters are used in the numerical simulations for electrons, at a temperature of 300 K and intrinsic doping. In these simulations, the transverse electrical field is the local one. It means it is derived for each point of the mesh, which is impossible to do in a compact model. Note that for the value of transverse field in a DG MOSFET, $E_\perp^{1/3}$ is negligible.

Moreover, carriers are accelerated by a lateral electrical field. Their velocity begins saturating when the field reaches a limit value. It is modeled by an equation which provides a smooth transition between low field and high field behavior [2].

3.2 Mobility model due to transverse electrical field

The mobility model should take into account same effects (phonons and surface roughness) but making them compact. To adapt this model to the independent double gate MOSFET, two mobility equations are necessary, one for the front and the other one for the back interface, μ_1 and μ_2. Besides, the mobility degradation due to the transverse electrical field is modeled thanks to front and back effective transverse electrical fields E_{eff1} and E_{eff2}. They are defined by:

$$E_{eff1} = E_{s1} + E_{cpl} \tag{3a}$$

$$E_{eff2} = E_{s2} - E_{cpl} \tag{3b}$$

where E_{si} is the front or the back surface field. *i* is an index: 1 for the front interface and 2 for the back one.

$$E_{si} = -\frac{Q_{invi}}{2\varepsilon_{ox}} \Rightarrow E_{si} = -\frac{V_{gsi}}{2T_{oxi}} \tag{4a}$$

$$V_{gsi} = 2u_t n_i \ln\left[1 + \frac{\exp\left(\frac{V_{gi} - V_{thi} - V_{offi}}{2u_t n_i}\right)}{1 + 2\exp\left(-\frac{V_{gi} - V_{thi}}{2u_t n_i}\right)}\right] \tag{4b}$$

V_{gsi} allows a continuous description from weak to strong inversion and V_{offi} is a correction factor describing the non total screening of the inversion layer in strong inversion. All parameters are explained in [3].

E_{cpl} is the coupling field characterizing the interaction between interfaces. This is the particularity of the presented model: thanks to E_{cpl}, which allows an accurate description of the transverse field when one interface is in weak inversion and the other one in strong inversion, the mobility model will be precise and physical.

To include (2) in our compact model, we define front and back mobility as:

$$\frac{1}{\mu_1} = \frac{1}{\mu_{01}} + \frac{1}{\frac{a_1}{E_{s1} + b_1 E_{cpl}}} + \frac{1}{\frac{c_1}{E_{eff1}^{2}}} \tag{5a}$$

$$\frac{1}{\mu_2} = \frac{1}{\mu_{02}} + \frac{1}{\frac{a_2}{E_{s2} - b_2 E_{cpl}}} + \frac{1}{\frac{c_2}{E_{eff2}^{2}}} \tag{5b}$$

μ_{0i}, a_i, b_i, c_i are fitting parameters. These new equations are introduced in our compact model instead of the constant mobility parameters.

3.3 Velocity saturation model

The carrier saturation velocity is an important effect that affects short channel transistors. When the lateral electrical field is high, the carrier velocity saturates at v_{sat}. The chosen model is adapted from [5] defining two saturation fields E_{sat1} and E_{sat2}:

$$E_{sati} = 2\frac{v_{sati}}{\mu_i} \tag{6}$$

where v_{sati} is the saturation velocity, which is a fitting parameter. E_{sati} is included in the saturation drain voltage V_{dsati} given by:

$$V_{dsati} = n_i \frac{E_{sati} L\left(V_{gi} - V_{thi} + 2u_t\right)}{E_{sati} L + \left(V_{gi} - V_{thi} + 2u_t\right)} \tag{7}$$

n_i is the coupling factor, also defined in [3]. Finally, V_{dasti} is included in the drain current equation of our compact model [1].

$$I_{ds} = I_{ds1} + I_{ds2} \tag{8}$$

4 RESULTS

This model was confronted to ATLAS numerical simulations with the CVT-Lombardi model [2]. As reported in the previous section, model and simulation assumptions are the same. The silicon thickness is 10 nm and the front and the back gate oxide thicknesses are 1 nm.
Results are shown in Figs 3 to 10. Figs 3 to 5 are for a long channel MOSFET (130 nm). Drain current for different voltages are drawn showing an excellent matching between the developed model and the numerical simulations.

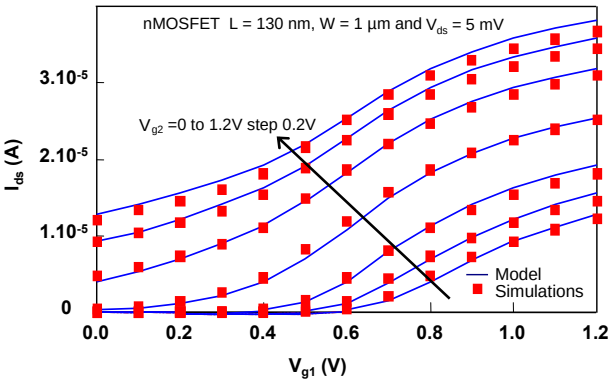

Figure 3: Drain current of a 130 nm gate length transistor versus front gate voltage for different back gate voltages (from 0 V to 1.2 V) in linear scale, in linear regime for a drain voltage of 5 mV.

Fig. 3 presents the drain current versus the front gate voltage for different back gate voltages in linear regime and in linear scale whereas Fig. 4 illustrates the same characteristics in saturation regime and in logarithmic scale in order to prove the accuracy of the developed model whatever the operating mode.

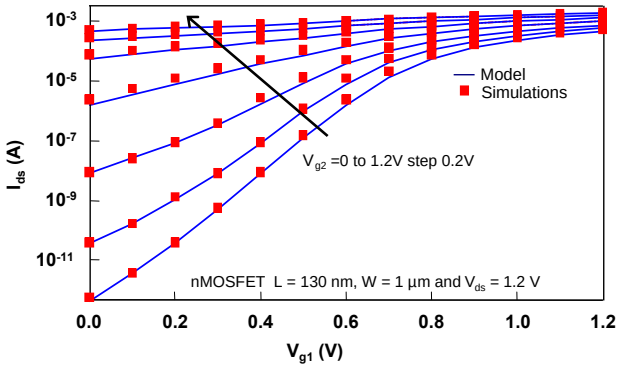

Figure 4: Drain current of a 130 nm gate length transistor versus front gate voltage for different back gate voltages (from 0 V to 1.2 V) in logarithmic scale for a drain voltage of 1.2 V.

Fig. 5 shows the drain current versus the drain voltage. It is also well modeled whatever the front drain voltage. It means that the coupling field is well taken into account in the carrier mobility model.

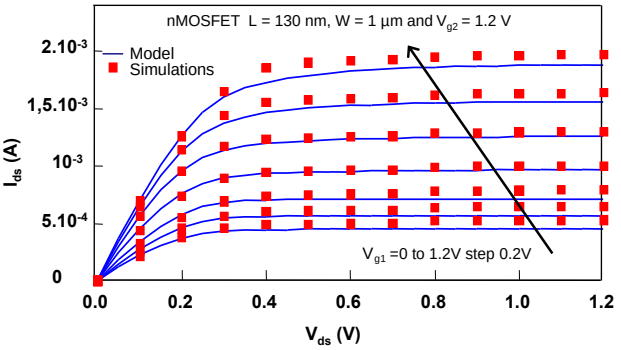

Figure 5: Drain current of a 130 nm gate length transistor versus drain voltage for different front gate voltages (from 0 to 1.2 V) for a back gate voltage of 1.2 V.

Figs. 6 to 10 are for a short channel MOSFET (30 nm). Same figures as for a long channel are shown.

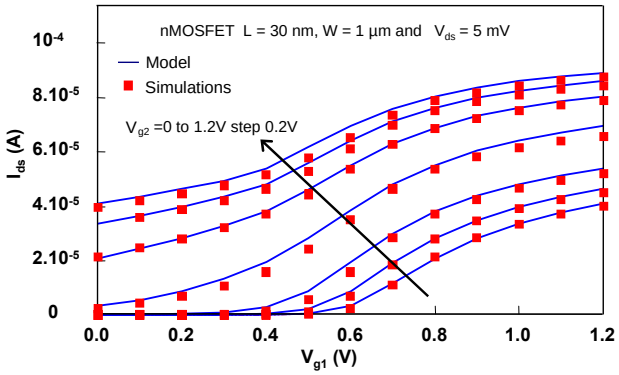

Figure 6: Drain current of a 30 nm gate length transistor versus front gate voltage for different back gate voltages (from 0 to 1.2 V) in linear scale for V_{ds}=5 mV.

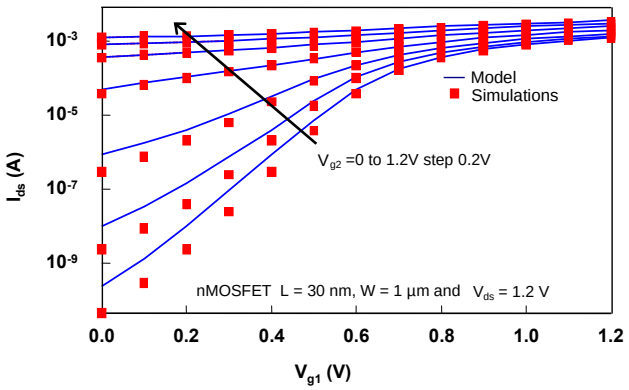

Figure 7: Drain current of a 30 nm gate length transistor versus front gate voltage for different back gate voltages (from 0 to 1.2 V) in logarithmic scale for V_{ds}=1.2 V.

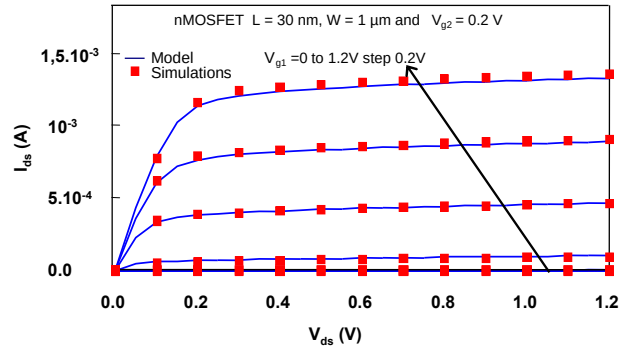

Figure 8: Drain current of a 30 nm gate length transistor versus drain voltage for different front gate voltages (from 0 to 1.2 V) for a back gate voltage of 0.2 V.

Very good results are also obtained. Only in weak inversion at both interfaces and in saturation regime the model is less exact. The front gate transconductance and the drain conductance are also displayed on Figs. 9 and 10. They prove that not only the drain current matches well the numerical simulations, but also the derivatives.

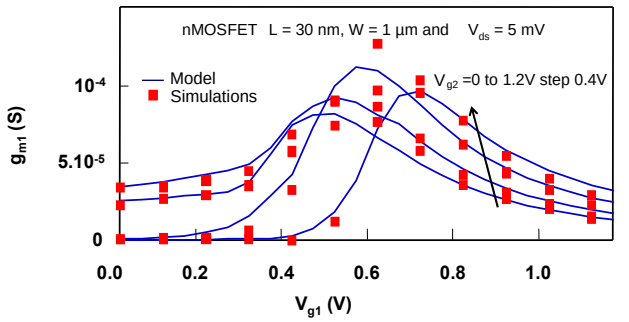

Figure 9: Front gate transconductance of a 30 nm gate length transistor versus front gate voltage for different back gate voltages (from 0 to 1.2 V) for V_{ds}=5 mV.

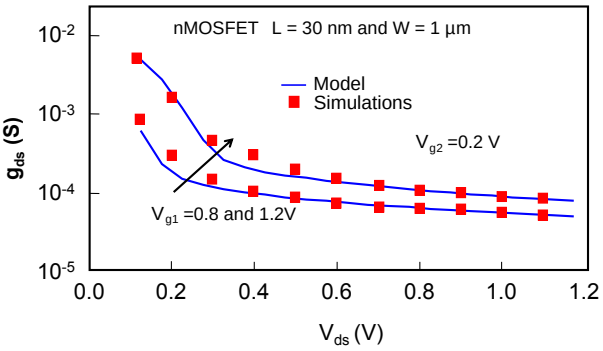

Figure 10: Drain conductance of a 30 nm gate length transistor versus drain voltage for different front gate voltages for a back gate voltage of 0.2 V.

5 CONCLUSION

An explicit threshold voltage based compact model of IDG MOSFET with a physically-based carrier mobility model is presented. This model takes into account the transverse electrical field as well as the velocity saturation. The mobility degradation due to the transverse electrical field model is adapted to the independent double gate MOSFET thanks to the inclusion of a coupling field between both interfaces. That is why whatever the operating mode (weak /weak, weak/strong or strong/strong inversion), the mobility model is adapted to the IDG MOSFET.

Confrontations with Atlas simulations prove its excellent accuracy for a long and a short channel device whatever the polarization.

Another interest of this model is that different mobility models can be implemented at each interface.

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