

Pre-Distortion Assessment of Workfunction Engineered Multilayer Dielectric Design of DMG ISE SON MOSFET

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In order to overcome device miniaturization roadblock in sub-100 nm regime, innovative architectural enhancements involving the use of an improved SOI like architecture called Silicon On Nothing (SON) capable of SCE and DIBL suppression [1] onto the existing ISE devices [2], has been considered for SCEs suppression. Further to overcome the electron transport inefficiency [3], Dual Material Gate (DMG) architecture has also been integrated thereby presenting ultimate device architecture of DMG ISE SON for ULSI era. In RF applications minimization of third order intermodulation (IMD3) is vital as it generates harmonics close to the desired signal and cannot be cancelled by push-pull configuration as for second order distortion. In this work, linearity performance of 50nm DMG ISE SON MOSFET as shown in Fig. 1, has been investigated and compared with other Single & DMG taking into consideration the non-equilibrium transport effect implemented via EBT-model activated through ATLAS-2D device simulation software. The work discusses the linearity Figure of Merits -VIP₂, VIP₃ and IMD3 and thereby, provides optimal bias point selection. In order to explore the linearity performance, transconductance g_m as well as the higher order derivatives g_m' & g_m'' as shown in Fig. 2 is studied. g_m is low in the subthreshold region and then rises to a peak between 0.9 and 1.0V, for all devices under consideration. The value of g_m' & g_m'' are found to be lowest around V_{GS} of 0.9-1.0V & 0.6-0.7V respectively for all devices under consideration. The nonlinearity exhibited by these higher-order derivatives of $I_{DS}-V_{GS}$ characteristics determines a lower limit on the distortion and therefore, the amplitude of g_m' & g_m'' should be minimum and from Fig. 2, lowest value where a dip in g_m' & g_m'' , are seen for DMG ISE SON. However, gate bias of 0.6V is preferred as at this bias point, g_m'' crucial for improved linearity, attained a minima. Fig. 3 & 4 gives the variation of VIP₂ ($VIP_2 = 4 \frac{g_m'}{g_m}$) and VIP₃

($VIP_3 = \sqrt{24 \frac{g_m''}{g_m}}$) with V_{GS} for all the structures. It is seen that VIP₂ peak is highest for DMG

ISE among all devices. However, with thinning of channel film (T_{film}), VIP₂ value improves significantly for DMG ISE SON. For the same electrical gate length as SMG ISE, DMG ISE SON exhibits a considerable enhancement in VIP₂ but is lower than DMG ISE and DMG SON. The VIP₃ peak, signifying the second order interaction effect reflecting the cancellation of third-order nonlinearity coefficient by device internal feedback around second-order nonlinearity as shown in Fig. 4, in DMG ISE SON is appreciably higher than the other MOSFETs. The lower gate bias ($V_{GS}=0.6V$) is desirable as at this biasing condition considerably higher value of g_m is obtained as compared to the values obtained at higher gate bias ($V_{GS}=1.4-1.6V$). It further implies that a lower gate drive is required to preserve linearity. Thus, DMG ISE SON is more linear than other counterparts.

[1] Monfray et al., *IEDM Tech. Digest*, pp. 645, 2001.

[2] R. Kaur et al., *IEEE Trans. on Electron Devices*, Vol. 54, No.2, pp. 365, February 2007.

[3] W. Long and K. K. Chin, *IEDM Tech. Digest*, pp. 549, 1997.

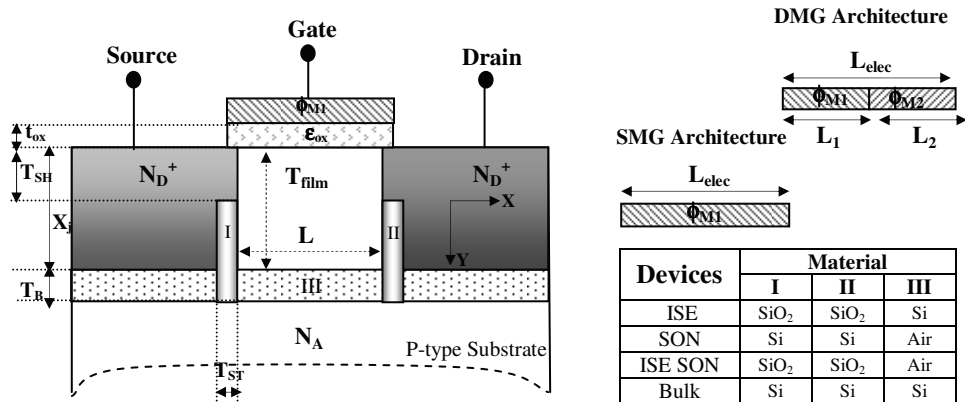


Fig. 1 Schematic cross section of various MOSFET structure under consideration. $L_1 = 50$ nm, $T_{ST} = 10$ nm, $T_{SH} = 10$ nm, $T_{VH} = 75$ nm, $T_{film} = 30$ nm, $T_B = 10$ nm, $X_j = 30$ nm, $t_{ox} = 3$ nm, $N_A = 1 \times 10^{17}$ cm⁻³. Work function - $q\phi_{M1} = 4.77$ eV & $q\phi_{M2} = 4.71$ eV.

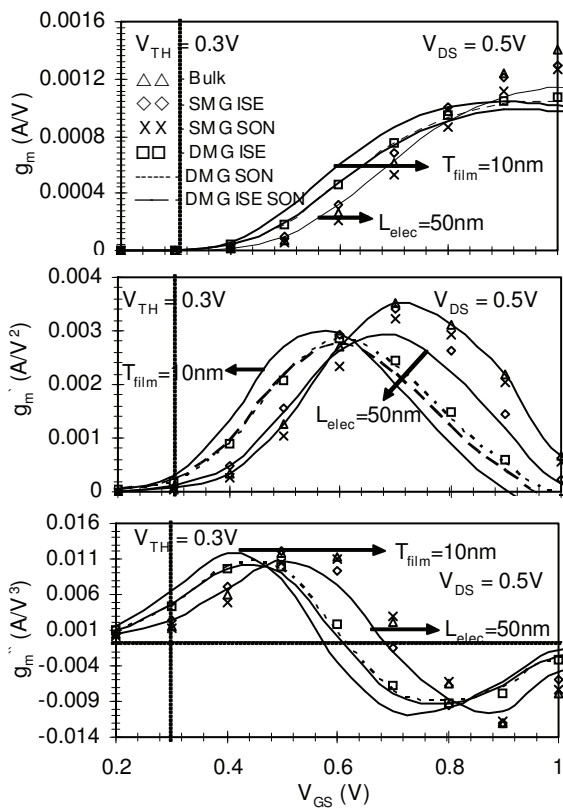


Fig. 2 Simulated (g_m), (g_m') & (g_m'') Vs V_{GS} characteristics for various MOSFETs. $V_{DS} = 0.5$ V, $L = 50$ nm, $W = 1 \mu$ m, $\epsilon_{ox1} = 3.9$, $T_H = 10$ nm, work function ($q\phi_{M1}$) = 4.77 V for SMG and for DMG, ($q\phi_{M1}$) = 4.77 eV and ($q\phi_{M2}$) = 4.10 eV.

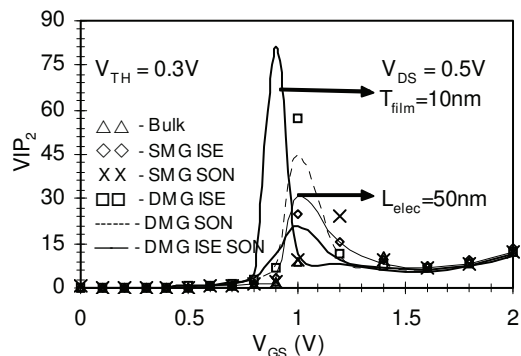


Fig. 3 VIP_2 variation with V_{GS} for various DMG and SMG MOSFETs. $L = 50$ nm, $T_H = 10$ nm, $T_S = 20$ nm, $\epsilon_{ox1} = 3.9$, $q\phi_{M1} = 4.77$ eV, $q\phi_{M2} = 4.10$ eV and $V_{DS} = 0.5$ V.

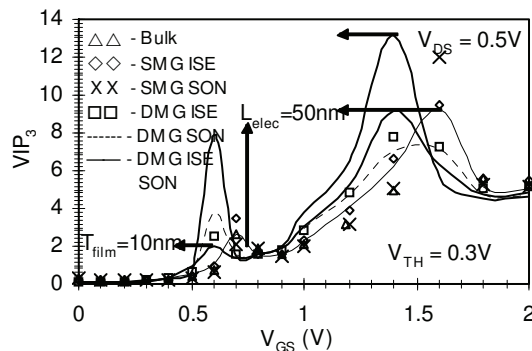


Fig. 4 VIP_3 variation with V_{GS} for various DMG and SMG MOSFETs. $L = 50$ nm, $T_H = 10$ nm, $T_S = 20$ nm, $\epsilon_{ox1} = 3.9$, $q\phi_{M1} = 4.77$ eV, $q\phi_{M2} = 4.10$ eV and $V_{DS} = 0.5$ V.