Test ASIC for Real Time Estimation of Chip Temperature

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ABSTRACT

The main goal of this paper is to present the design and operation of an ASIC, which will be used in the research devoted to the development of a real time temperature monitoring system. This circuit will serve two major purposes: gathering information necessary for the conception of sensor placement strategies and the elaboration of robust algorithms for the real time estimation of the circuit temperature as well as the practical verification of the developed solutions.

The first part of this paper will be devoted to the detailed description of the entire ASIC design whereas the second part will present the operation of the circuit based on the computer simulations. The main aspects of proper layout preparation are also included.

Keywords: temperature monitoring, thermal modeling, ASIC

1 INTRODUCTION

The continuous increase of the operating frequency and the miniaturization of electronic circuits augmented the density of dissipated power, which led to the serious thermal problems, even in apparently low power applications. Thus, in order to protect electronic circuits from an overheating and also a destruction, thermal issues should be considered both in the circuit design phase as well as during its operation.

Nowadays, temperature differences in electronic circuits, especially those equipped with efficient cooling systems, can exceed several tens of degrees Kelvin. On the other hand, temperature very rarely can be measured directly where the heat is generated and the placement of a single temperature sensor at some location in the layout will not guarantee that the maximal temperature allowed is not exceeded elsewhere. Thus, there arises a need to devise more sophisticated systems for real time temperature monitoring for overheat protection purposes, which would be based on remote sensor measurements. Such a system should be fast and reliable one but should not occupy too much surface.

2 CIRCUIT DESIGN

2.1 Chip Overview

The entire circuit was designed in the Department of Microelectronics and Computer Science (DMCS) at the Technical University of Lodz. DMCS is one of the very few ASIC design centers in Poland, but at the same time it is the leading one and it has a long-term experience in the thermal and electro-thermal simulation of electronic devices and systems.

The entire circuit was designed in the CADENCE environment and the AMS (AustriaMicroSystems) 0.35 um HV technology, which offers a possibility of combining the standard 3.3 V CMOS logic circuits with the 50 V power MOS transistors. The ASIC consists of the following two main parts:

- analog – a heat source and temperature sensor matrices,
- digital – a control unit, data processing units and a static RAM.

These parts are described in next sections of the paper.

2.2 Analog part

The analog part of the chip is responsible for the heat generation and temperature measurements. It consists of such elements as temperature sensors, heating transistors, comparators, current mirrors and overheating sensor. The heat generation is realized with NMOS High Voltage (HV) transistors. Each heating transistor is the NMOS one with the V_{DS}=50 V and maximal current I_{DS}=21 mA. There is a possibility to adjust the current of each power transistor (circled in Figure 2) with the aid of the three-step current mirror. As temperature sensors, diodes made by proper connection of bipolar transistors are used. Three diodes connected in series are one of the temperature sensors. The output voltage from the temperature sensor is given to the input of a comparator. The comparator with the counter creates a simple ADC. The analog signal from the temperature sensor is converted to the digital one. Next step is processing obtained data with usage digital blocks and finally send it to a PC computer.

In the test chip, 25 temperature sensors are placed near the heat transistors. The idea of placing these sensors is

shown in Figure 1. Such a sensors location allows for monitoring the silicon temperature that is dissipated by power transistors as near the heat source as possible.

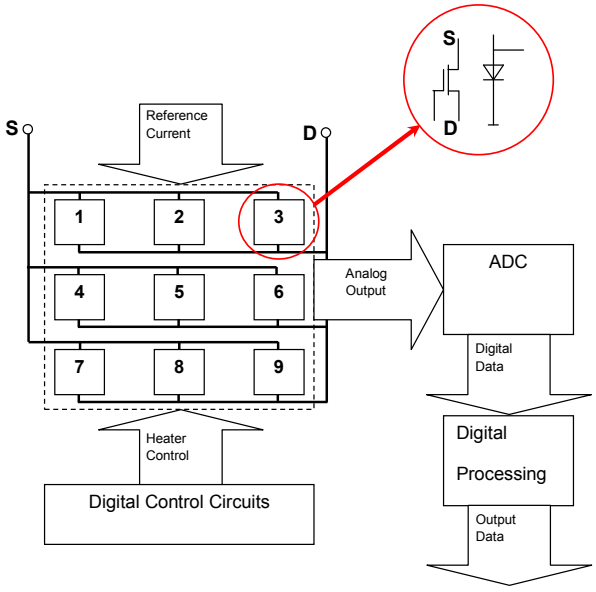

Figure 1. ASIC Block Diagram

Moreover the analog output of each temperature sensor is led out outside the chip to verify the proper processing in the digital part of a chip.

2.3 Digital part

The digital part of the circuit was described as the VHDL code, which was synthesized then to schematics using the tools built into the Cadence environment. Then, the layout was obtained in a fully automatic way with the standard place and route tools. The digital part contains circuits that realize the following functions:

- control of the heat source power dissipation,
- A/D conversion of temperature sensor signals,
- acquisition of measurement data,
- communication with the environment.

The memory of a given size and aspect ratio was synthesized by the manufacturer and provided as a kind of a 'black box'. The main purpose of this memory is to store the measured data, coefficients of digital filters and the temperature estimation results in the real time operation mode of the circuit.

The circuit was designed to work in two modes: the measurement mode and the estimation mode. In the first one, power is dissipated in the circuit and all the signals from the temperature sensors are sent to some external circuits for storing and further processing. In the second mode, the measured data converted to the digital signal will be processed on-chip by the digital filters to produce real time circuit temperature estimates.

The first mode will be used for the investigations aimed at the optimization of circuit thermal model and topology as well as the development of algorithms for real time temperature estimation. Then, all the proposed solutions will be implemented in the chip and thoroughly verified in practice using the second operating mode.

In Figure 4, the block diagram of the digital control unit is presented. It contains following parts:

- main calculation module with memory and control unit subcircuits,
- serial input/output from the main module,
- digital part of the ADCs,
- heat transistors control unit.

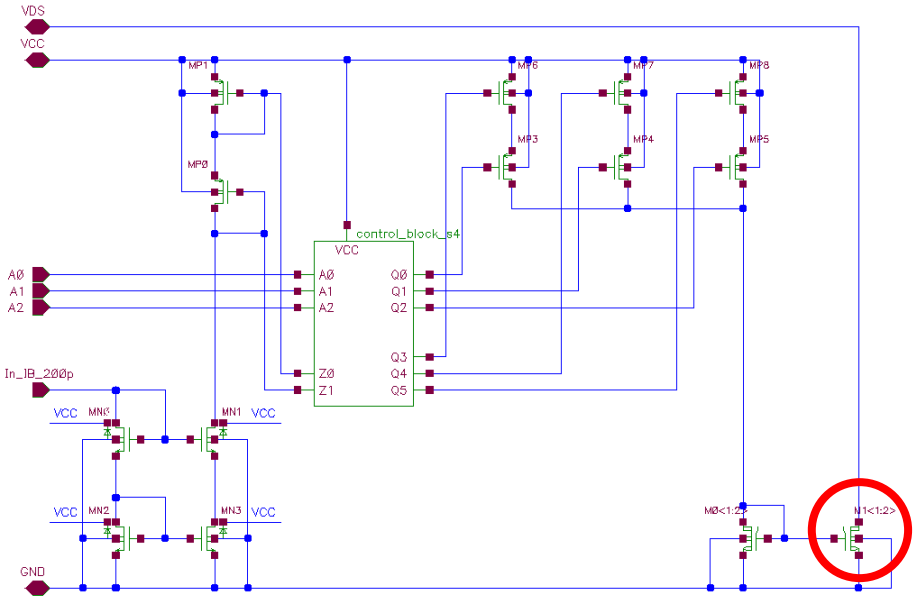

Figure 2. One Heat-Generation Cell Schematic

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3 SIMULATION RESULTS

The analog part of the chip, i.e. the heat sources and temperature sensors, was designed from a scratch as a full-custom circuit. The 9 heat sources, HV NMOS transistors, were arranged in a 3x3 matrix. The sources can be switched on and off independently at prescribed power dissipation levels as illustrated in Figure 3 (current levels with multiplication of V_{DS}=50 V). The local chip temperature can be measured with diodes, which are placed in the middle of each heating transistor and close the edges of the chip in 16 other locations marked with circles in Figure 5. The 1 mA forward current flows through each diode, what makes possible to obtain the measurement sensitivity
of -1.5mV/K. The voltage signals of each diode can be simultaneously read on the ASIC pins for sensor calibration and method testing purposes.

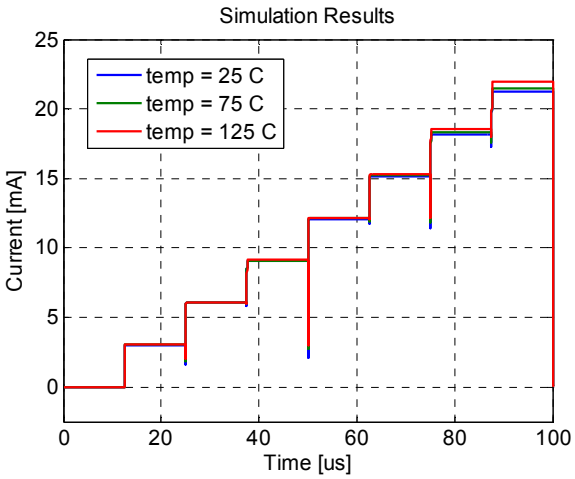

Figure 3. Heat Source Current Levels

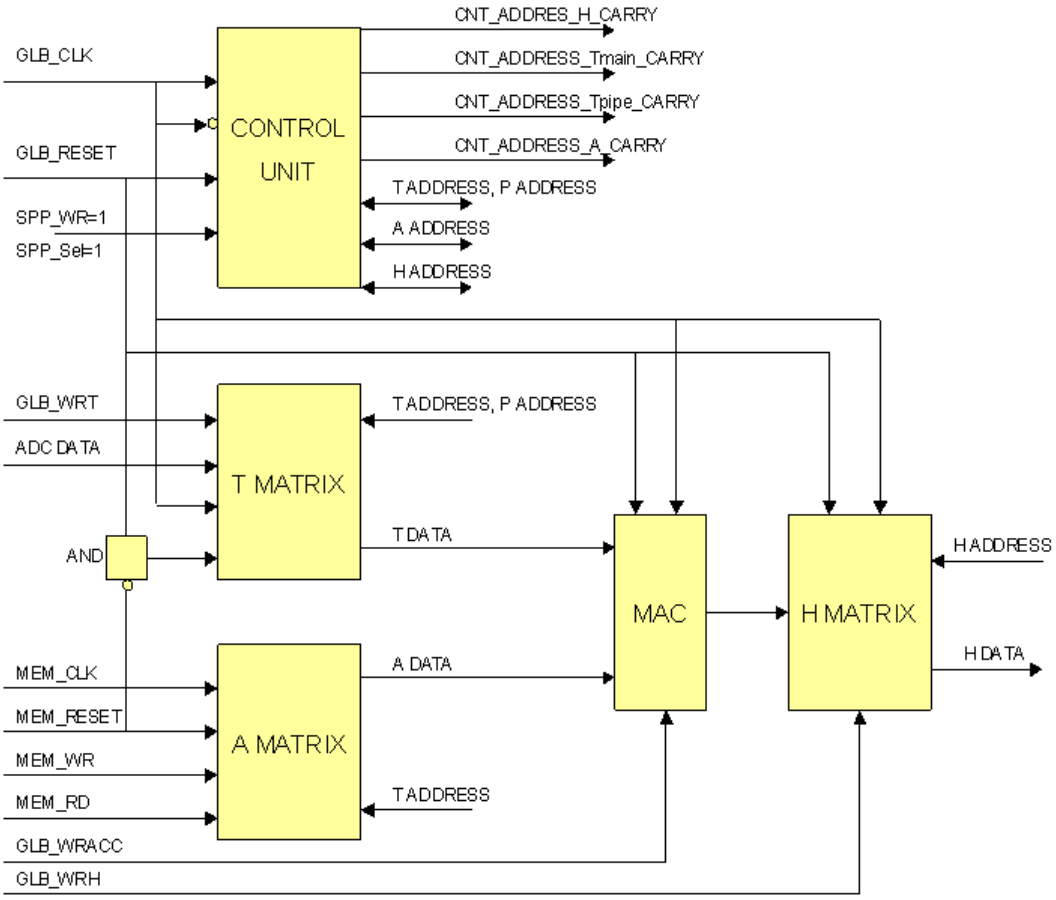

Figure 4. Block Diagram of the Digital Control Unit

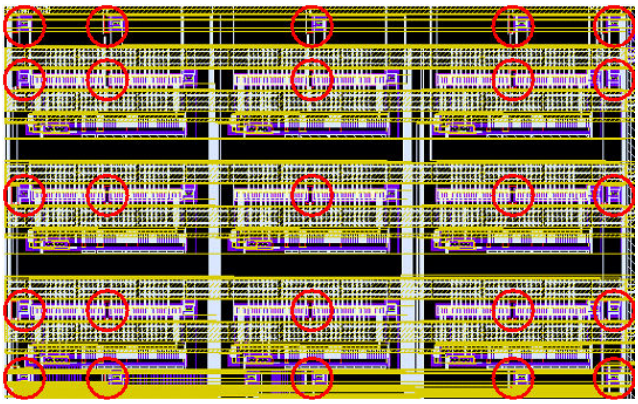

Figure 5. Analog Part Layout
with Marked Temperature Sensors

Due to long time of designing layout and waiting for the manufactured chip, the full verification of the simulations against the measurements is not presented in this paper but will be certainly presented during the conference.

4 LAYOUT

The full test chip layout is presented in Figure 6. The ¾ of the total core area is occupied by the analog part (heat transistors and temperature sensors). To minimize the influence of the analog part on the digital one and vice versa, each block is saved by guard ring. They reduce the disturbances profoundly. The total chip area is about 20 mm^2.

The size of the analog core part, i.e. without pads and digital blocks (simplified floor plan is shown in Figure 5), is 2 mm × 3 mm.

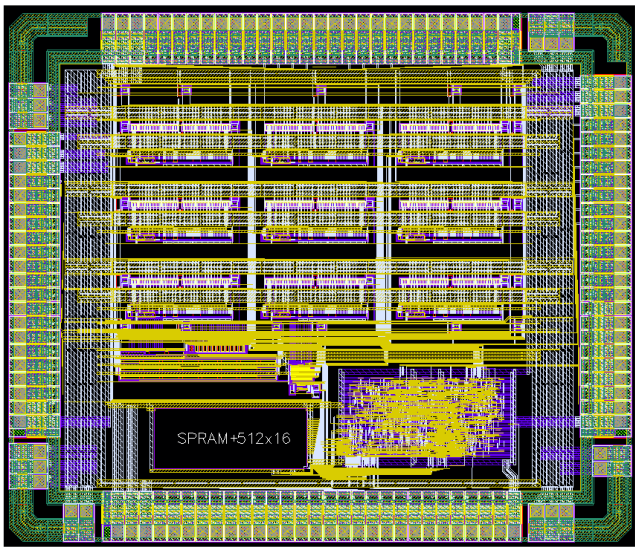

Figure 6. Chip Layout

The entire design of the circuit is currently being finished and was sent for manufacturing. The packaged chips should be delivered till the end of April. This should allow the full evaluation of the design.

5 CONCLUSIONS

In this paper the test ASIC for the temperature monitoring was presented. The power transistors located in a 3×3 matrix generate proper heat, that is measured with usage of diodes. There are two kinds of processing data from sensors: direct output from the chip or send them to the digital processing unit that calculates all necessary information. This approach allows the authors to choose proper temperature sensors location inside the chips that needs temperature-monitoring system.

6 ACKNOWLEDGEMENTS

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