Process Sensitivity Analysis of a 0.25-μm NMOS Transistor Using Two-Dimensional Simulations

Abdol A. Keshavarz*, Laurent F. Dion*, Pierre C. Leonardi**
* Reliability and Process Control Department, STMicroelectronics, Phoenix, AZ
** Device Engineering Department, STMicroelectronics, Phoenix, AZ
Phone: (602) 485-2925, Fax: (602) 485-2925, Email: abdol.keshavarz@st.com

ABSTRACT

The purpose of this work is to present an accurate simulation of the effects of major process changes on some of the most important device parameters of a 0.25-um NMOS transistor. The approach predicts the effects of several critical process steps including poly CD (channel length), threshold-voltage implant, NLDD implant, N+ Source/Drain (S/D) implant, and the final RTA thermal budget on the 0.25-μm NMOS device parameters. Results can be used for the fine-tuning of the device, and its parameter variations as a result of process changes. The modeling approach can reduce expensive and time consuming experiments for device improvements. The simulation model proves to predict accurate results and is currently used for more investigation of the 0.25- μm NMOS Transistor in STMicroelectronics site in Phoenix, AZ.

Keywords: NMOS 2D-simulation, 0.25-μm NMOS, Sensitivity Analysis, Process Effects on 0.25-μm NMOS

1. Key Process Features

CMOS devices are built on N-epi, use shallow trench isolation (STI), and the process utilizes twin-tubs with retrograde wells. Double poly with salicidation on poly and junctions (N+ and P+) are used and the oxide thickness is 50 Angstroms. NMOS source and drain structures receive only Arsenic implants (no Phosphorus). This purpose is to make the device more robust, especially with respect to thermal budget changes. The anti-punch-through implant dopant is Indium, a large-atom dopant that is stable and with minimum diffusion, a critical factor for the short channel device. Only the NMOS is addressed in this work. This device is part of the 0.25-μm technology in STMicroelectronics that utilizes both MOS and Bipolar devices.

2. Methodology

0.25-mm transistors were developed and published in late 80's and early 90's, [1]-[3], with technology features and characterization results. Subsequently, the application of this transistor in the newly developed products showed up [4], [5]. Parallel to the technology development, simulation tools also had to improve to include the new necessary features. These included an overall improvement of the models covering the heavy-ion implant models (In), and accurate simulation of the effects of Arsenic and Indium implants on boron diffusion. This illustrates only some of the challenging problems to be solved before the accurate simulation of the 0.25-μm device was possible.

In this work, two-dimensional process and device simulation tools (ISE from Synopsys [6]) that have advanced Models to address all of the above were used for this work. Latest process simulation models (implant/ diffusion) available in the simulation tool were utilized for this purpose [7]. For Indium profile, Monte-Carlo method was used for highest level of accuracy. For the device simulation part, the accurate mobility models that are crucial for the accuracy of the results (mobility dependence on doping density, saturation velocity, and normal electric field) were used [8]. For the calibration of the results, only gate poly work function was adjusted. Very good agreement between the experimental and the simulated results was seen on the linear, sub-threshold, and saturation regions of the device.

Subsequently, a selected number of major device parameters were extracted from the simulation results. These included the threshold voltage (Vth), saturation current (IdSat), linear current (IdLin), sub-threshold slope (Subth), maximum transconductance (Gmax), device resistance in the linear region (Rlin), and output conductance in saturation region (Gds). Accurate process recipes used for the manufacturing of the 0.25-μm NMOS were used for the simulations.

3. Results and Discussions

Figure 1 shows the main part of the two-dimensional simulated structure as produced by the process simulator. Figures 2 and 3 show the comparison of the simulation and the experimental results (Data) for the major NMOS characteristics. Selected wafer was close to the targets based on all electrical parameters measured in line. Experimental data for the linear region of the device showed some variations on different measured sites, so two measured curves (lowest and highest measured currents) were provided for this region. The simulated sub-threshold region showed very good match to the

data, too. Same level of agreement was seen on the saturation region. No optimizations were done to improve the curves in this region. The good agreement between the measured data and the simulation seen on these figures strongly supports and validates the simulation approach.

Table 1 is the summary of the main results. Device parameters and their simulated baseline values are included. The selected process steps, their baseline values and their shifts used for sensitivity analysis are

shown too. The simulated change for each device parameter in response to the specified process shift is included.

Overall results indicate that the device is stable with respect to process changes, which is a desirable result. This is in fact expected from the all-Arsenic S/D and its low diffusion coefficients. But changes in poly CD (gate length) are considerable and calculated effects are presented. Effects of threshold-voltage implant (dose and energy) are included too. RTA time variation shows some effects, but it is not significant.

Results for the effects of channel length on device parameters are shown in Figures 4 and 5. These include simulated linear region characteristics, maximum transconductance (Gm), the saturation region characteristics, and the output conductance of the device for different channel lengths.

4. Conclusions

The two-dimensional simulation model is in very good agreement with experimental data. It is a valuable tool for the analysis and improvement of the 0.25-μm NMOS performance. Results indicate that the device is robust and stable with respect to a number of process changes. Poly CD change is the most dominant variable affecting the device parameters. This is an ongoing project and the model is actively being used.

References

[1] W. Chang, B. Davari; M. Wordeman; Y. Taur, C. Hsu, M. Rodriguez, "A high-performance 0.25-μm CMOS technology. I. Design and characterization", IEEE Trans. on Electron Devices, Vol. 39, Apr 1992.

[2] B. Davari, W. Chang, K. Petrillo, C. Wong, D. Moy, Y. Taur, M. Wordeman, J. Sun, C. Hsu, M. Polcari, "A high-performance 0.25-μm CMOS technology. II. Technology", IEEE Trans. on Electron Devices, Vol. 39, Apr 1992.

[3] B. Davari; W. Chang; M. Wordeman; C. Oh; Y. Taur; K. Petrillo; D. Moy; J. Bucchignano; H. Ng; M.. Rosenfield; F. Hohn; M. Rodriguez, "A high performance 0.25 μu m CMOS technology", IEDM Conference Digest, 1988, pages 56-59.

[4] S. Wuu, D. Yaung; C. Tseng; H. Chien; C. Wang, H. Yean-Kuen ; B. Chang, "High performance 0.25-um CMOS color imager technology with non-silicide source/drain pixel", Electron Devices Meeting, 2000.

[5] E. Zervakis, N. Haralabidis, "A fast 0.25um CMOS current-mode front-end stage for solid state detector interfaces", 9th International Conf. on Electronics, Circuits and Systems, 2002. Vol. 1, Page(s): 243- 246.

[6] Sentaurus Work Bench y-2006.06 from Synopsys, Inc.

[7] ISE TCAD Release 10.0, Vol. 2a Process Simulation, Part 8 Dios, Chapter 9 (Implantation), and 10 (Diffusion).

[8] ISE TCAD Release 10.0, Vol. 4a Device Simulation, Chapter 8, Mobility Models.

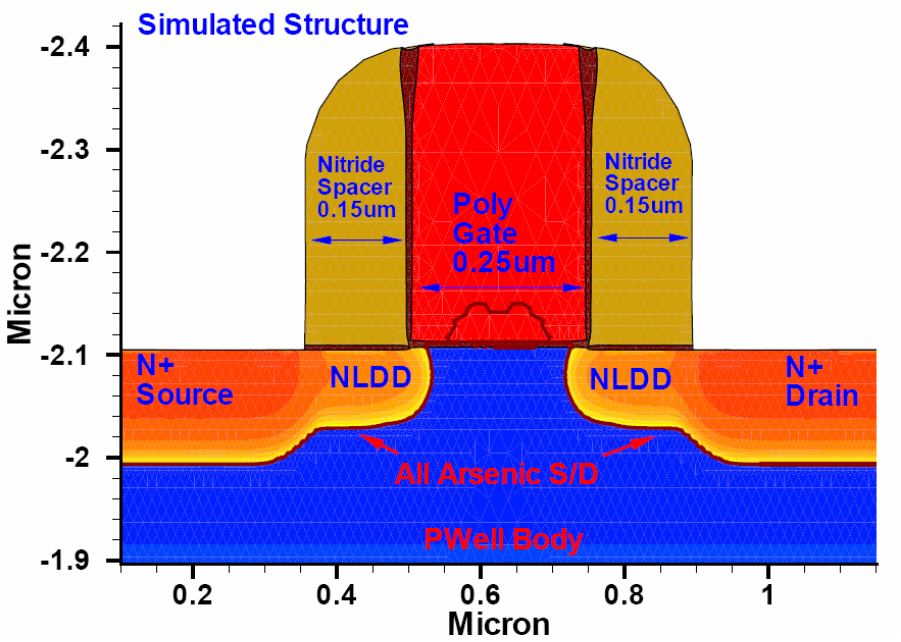

Figure 1. The two-dimensional simulated 0.25μm NMOS.

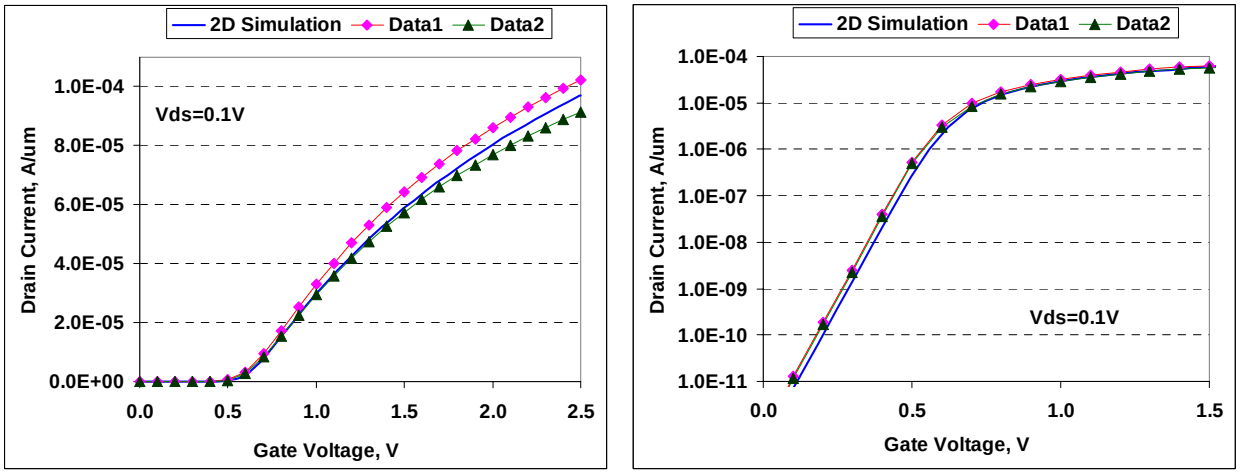

Figure 2. Simulated vs. measured results for the linear and the subthreshold regions.

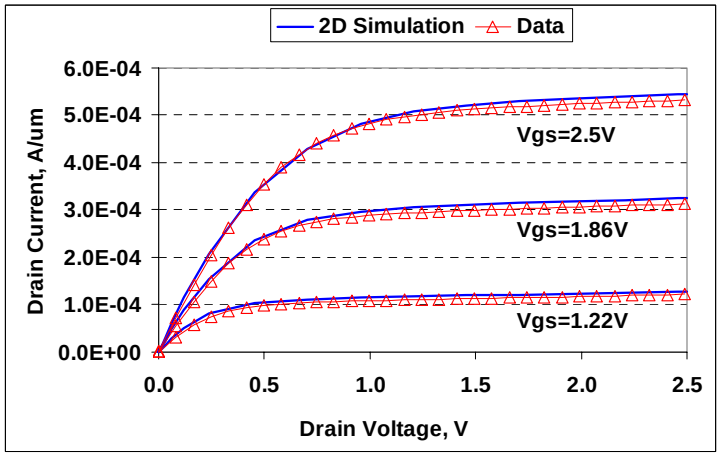

Figure 3. Simulated vs. measured results for the saturation region.

	Device Parameter Name →		VTh, mV	Rlin, Ohm.mm	IDLin, A/mm	Gmax, A/V	IDSat, A/mm	Gds, A/V	Subth, mV/dec
	Parameter Base Value →		550	1029.9	9.7E-05	7.8E-05	5.5E-04	1.7E-02	86.5
Steps Selected for Analysis	Nominal Value	Process Shift ↓	↓ Device Parameter Shifts ↓						
			mV	Ohm	A/um	A/V	A/um	A/V	mV/dec
Channel Lengh	0.25 um	0.05 um	73.86	226.3	-1.7E-05	-2.0E-05	-1.4E-04	-2.9E-03	2.74
Vth Implant Dose	7.0E12 cm-2	0.3E12	10.11	-12.0	1.1E-06	-8.0E-07	-7.0E-06	-2.5E-04	0.15
Vth Implant Energy	20 kev	5 kev	-44.95	-56.3	5.6E-06	4.5E-06	3.3E-05	8.5E-04	-1.52
NLDD As Implant Dose	3.0E14 cm-2	0.5E14	0.81	-29.4	2.9E-06	1.5E-06	7.7E-06	4.8E-04	-0.01
NLDD As Implant Energy	50 kev	5 kev	-1.40	1.6	-1.5E-07	6.1E-07	3.8E-06	8.4E-05	0.01
NPLUS As Implant Dose	3.80E+15	0.3E15	0.05	1.1	-1.0E-07	2.5E-08	1.5E-07	5.3E-06	0.00
NPLUS As Implant Energy	60 kev	5 kev	-0.85	-0.1	1.2E-08	-1.7E-07	-7.7E-09	2.3E-06	-1.87
S/D RTA Anneal	1048 C/20 sec	5 sec	2.93	1.2	-1.1E-07	4.4E-08	6.3E-07	3.4E-05	-1.04

Table 1. Simulated device baseline parameter values and their shifts in response to process changes.

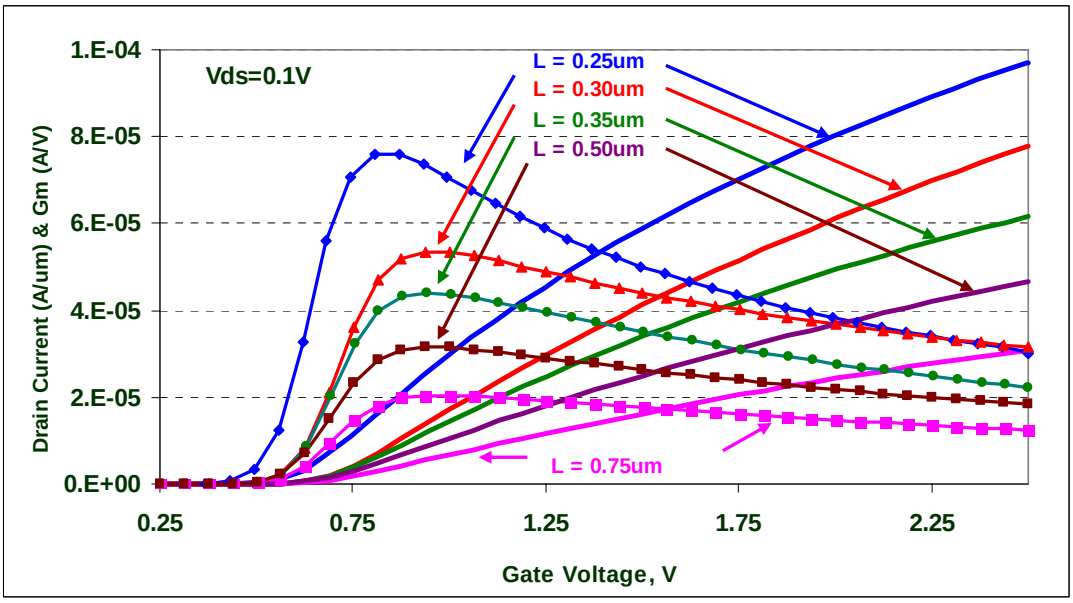

Figure 4. Simulated results for the device linear region for different channel lengths.

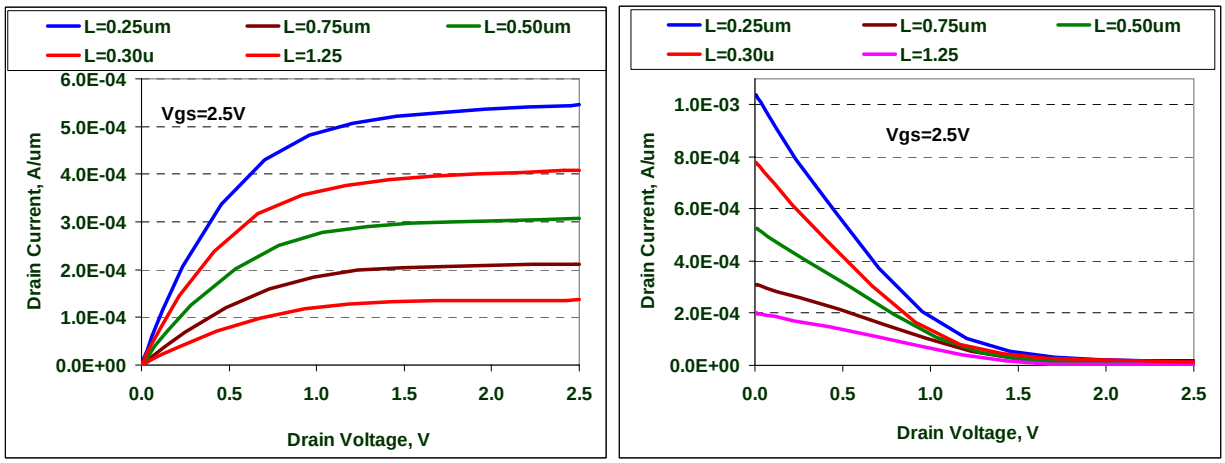

Figure 5. Simulated results for the device saturation region for different channel lengths.

NSTI-Nanotech 2008, www.nsti.org, ISBN 978-1-4200-8505-1 Vol. 3