3D Nanostructured Silicon Relying on Hard Mask Engineering for High Temperature Annealing (HME-HTA) Processes for Electronic Devices

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ABSTRACT

A 3D nanostructuration of silicon through hard mask engineering and high temperature annealing (HME-HTA) in hydrogen ambiance is reported The use of a nitride/oxide double hard mask stack on silicon during the etching of bulk structures allows for leaving a patterned nitride thin film on the structures surface during the high temperature annealing, after having removed the top oxide layer. This solution will be referred as the *nitride-capped approach*, which is an alternative to the use of a single sacrificial oxide hard mask for a free Si surface annealing (referred as the *mask-less approach*). The nitride-capped approach opens new technological and design possibilities when using 2D arrays of various geometry trenches. Implications and potential device applications are discussed, such as the role played by the silicon-nitride interface during the annealing process, the role of the remaining nitride layer, and the possibility to explore this 3D technique to solve the planar independent double gate transistor challenge.

Keywords: Silicon reflow, hydrogen annealing, 3D nanostructures, hard mask, autoaligned devices

1 SILICON REFLOW

Annealing silicon at high temperatures in a hydrogen ambiance has been reported to induce surface diffusion of silicon [1]. The result of such process at low pressure and high temperature on an etched cylindrical trench is the formation of a buried cavity within the bulk substrate (Figure 1a). By arranging these trenches in patterns like in a row or in a 2D matrix, these cavities can connect to each others if the initial trenches are close enough and will form a buried pipe or a buried planar cavity (Figure 1b). respectively

The use of a nitride hard mask for such a HTA process has been mentioned in [2] to remain stable during the HTA step. Moreover, it minimizes the surface diffusion at its interface with silicon. Indeed, it has been observed that the mechanism of cavity formation is different from nitride-capped structures compared to the case of a mask-less HTA. This observation has been confirmed by the mean of simulations in the frame of surface diffusion studies [3].

The deformation of the trench starts from its bottom, the nitride layer inhibiting the contribution of the upper part of the trench during the closing process, which normally plays

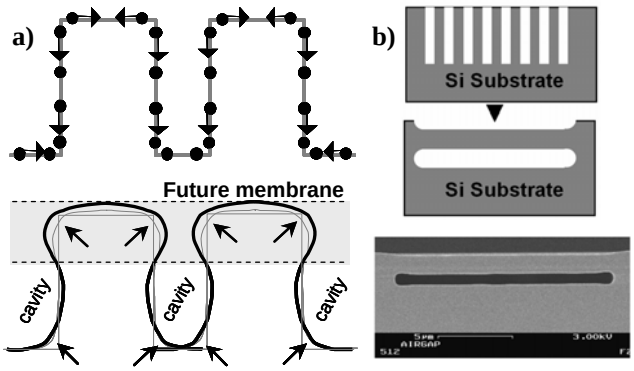

Figure 1: a) Surface diffusion during mask-less annealing: b) Example of a silicon membrane obtained with a H2 HTA

an important role in the cavity's formation mechanism (Fig 2). This is what enables the formation of multiple cavities for such trenches with a lower aspect ratio compared to the mask-less configuration.

Nevertheless, to the best of our knowledge, the behavior at the nitride-silicon interface has not really been taken into account yet. In cited papers, the main object of interest was the possibility for formation of multiple cavities allowed by the use of the nitride layer. In simulations, in order to give morphological predictions of the shape of an annealed structure with a nitride hard mask, the nitride-silicon interface is defined by a blocked surface condition.

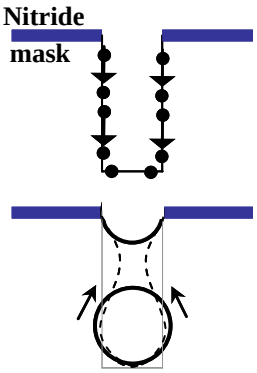

Figure 2: perfectly blocked nitride-silicon interface assumed during surface diffusion simulations.

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The work presented here intends to investigate the effects of a nitride hard mask on the hydrogen HTA of periodical structures, what has to our knowledge not been performed yet. In particular, we will see the role of the nitride-silicon interface on arrays of trenches and show what happens at this interface strongly influences the morphological results after annealing of the structures, and opens interesting possibilities for electronic devices fabrication.

2 EXPERIMENTS

2.1 Test wafers preparation

For this study, we compare two approaches, with: (i) a reference wafer annealed in hydrogen ambiance with a hard mask free surface (mask-less approach) and (ii) wafers annealed with a patterned nitride layer on the silicon surface (nitride capped approach). We used bulk wafers with two different types of hard masks for the silicon etching step:

- 3000Å TEOS hard Mask (mask-less annealing)
- 1600 Å Nitride hard mask deposited on Silicon
  3000 Å TEOS additional layer. (capped annealing)

Wafers for mask-less and nitride-capped approach have been through the same optical lithography and silicon etching steps. Before the annealing, the TEOS layer has been removed on both wafers. After an annealing at 1100°C during 10min with a pressure of 10Torr, SEM observations have been performed.

Observed patterns consist of 225µm^2 areas of circular trenches arranged periodically in matrices. Diameter (CD) of the circular trenches varies from 600nm to 1µm. As the largest trenches would take more time to eventually form a cavity compared to the smallest structures, we are able to make qualitative observations on the silicon diffusion dynamics by observing the different matrices.

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2.2 Observations

Observations on the reference wafer obtained with mask-less approach show that after annealing, adapted designs formed membranes as expected (Figure 3). Typical membrane and buried cavity thicknesses obtained are 1µm and 600nm, respectively. It should be noted that these dimensions are scalable by modifying the design of the matrices and by further processing of the membrane, like an oxidation/oxide etching step.

By comparing some annealed mask-less structures and nitride-capped structures, we observed that the silicon structure resulting of the annealing was almost equivalent: In Figure 4, we see single cavities about to contact each others to form the plate cavity. Moreover, the surface of the membrane can be considered planar in both structures, what was not supposed to be the case with the nitride-capped structures (Fig 4b). Notice that the dashed line traced in Fig 4a corresponds to the substrate surface (line out of observation plane), whereas the arrow markers are placed along the line corresponding to the remaining nitride surface (line in observation plane)

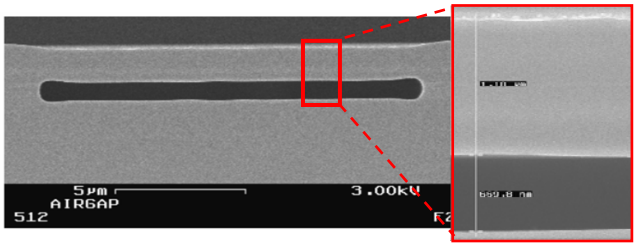

Figure 3: Buried cavity obtained after annealing of a trench matrix on the reference wafer (thicknesses: 1.10µm/669nm)

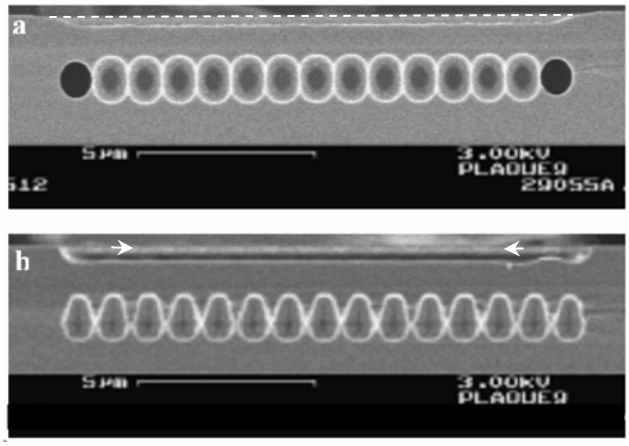

Figure 4: Same trench matrix processed with a) mask-less annealing b) nitride-capped annealing

We observed indeed on matrices with low Aspect Ratio (AR) and low density (AR=4.5, CD/Trench Spacing = 1), (Figure 5a), a profile close to the ones predicted by simulations in Figure 2, however, for higher densities and higher AR a different situation can occur.

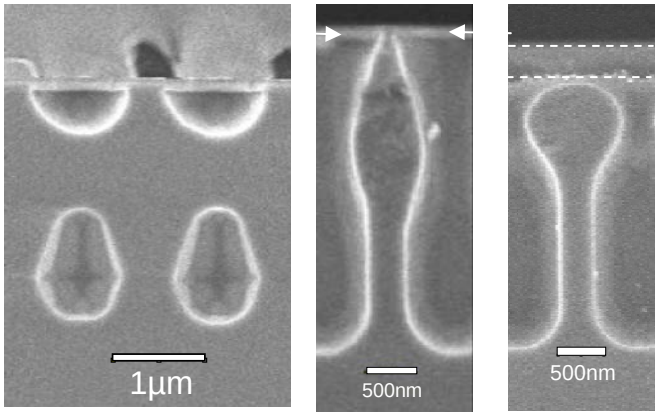

Figure 5: a) semi isolated trenches with hard mask after annealing b) annealed capped silicon trench wall in denser trenches array c) annealed mask-less silicon trench wall in denser trenches array, with ‘match shape’

We can see on Figure 5 b) that the trench wall between two trenches is about to detach from the nitride layer, indicated by the arrow markers. Indeed, at these temperatures, even if silicon tends to stay attached to the nitride layer, the surface diffusion of silicon occurring at the edges of the trench wall reduces more and more the surface of silicon in contact with the nitride layer. The contact area with the hard mask layer shrinks until the silicon detaches at some point. The trench wall is then supposed to be free to behave like the one in mask-less structures shown in Figure 5.c) In that mechanism, silicon in the area of the trenches matrix (lower dashed line) levels down compared to the initial substrate level (upper dashed line) and the walls between the trenches are shaping their profile in a 'match shape'

The non-spherical shape of the single cavities in Fig 5 b is explained by the interaction between the hard mask and silicon. Their shape is likely to evolve and to change to spheres like in the mask-less case, but after some additional time.

A suspended membrane can be obtained with both approaches, the interest in using a nitride mask is motivated by new geometrical features brought compared to the mask-less annealing process. Indeed, thanks to its stability and its structure, maintaining the nitride hard mask allows obtaining virtually two cavities (Fig. 6): one bottom closed cavity and one upper cavity delimited by the mask with built-in access (hard mask apertures). We have therefore the possibility to work on the membrane without etching new access.

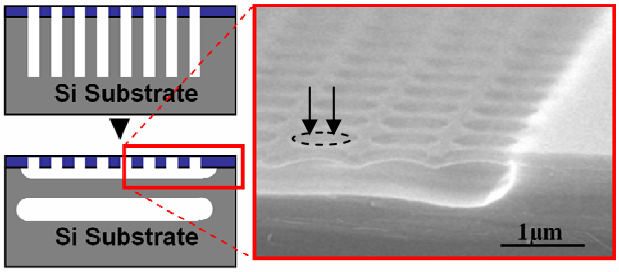

Figure 6: Annealing of nitride-capped structures allows obtaining two cavities -top and bottom-, considering the one delimited by the Si membrane surface and nitride layer.

3 PERSPECTIVES

3.1 3D structuration by HME-HTA as a novel engineering tool on bulk silicon

Based on the reported results, one can observe that the nitride capped approach offers a new tool for nanostructuration of bulk silicon and can be part of an interesting 3D Front End development. Combining design of cavities and etching, one can obtain a wide range of cavities heights and membranes thicknesses (still to be explored experimentally). Moreover, adjustments by processing are still possible, like the thinning of the silicon membrane by oxidation / oxide etching step mentioned in the mask-less approach and still available in this new configuration.

The interest of the remaining nitride layer is multiple: not only does it delimit the upper cavity, but it contains build-in access apertures for filling the upper cavity with a conformal material, and can as well be considered as a protective layer during the CMP process to planarize the deposited material. Nitride hard mask can as well simply be reused after the annealing step for its original function, ie a hard mask. Many trenches apertures geometries can lead to the same result we obtained during the silicon reflow step (like lines, but with a very high AR required, see [3]). A smart design of the mask apertures can be imagined so that the membrane and cavities formation is not disturbed during annealing, and yet the mask patterns can be used for a photolithographic step later in the process.

3.2 Application to the planar IDG transistor

The main challenges in realizing a planar independent double gate transistor are the alignment between the back gate and the front gate, and allowing contacting the two gates. Concerning the gate alignment issue, process with wafer bonding has shown good results with 10nm gate-length planar IDG transistors [5]. Some complex processes like in [6] relying as well on SOI substrates have been experimented

The HME-HTA nanostructuration allows obtaining two separated, superposed, autoaligned cavities. Each one of them can be processed separately to create a gate, being filled with different gate materials if necessary, as shown on Fig 7a). With such a technique, one can avoid wafer bonding. Of course, there is a main problem remaining: the bottom gate may be not isolated easily if working on a bulk substrate. However, simulations of mask-less structures annealing on SOI have been performed in [3] and the results show that one of the possible morphological configurations after annealing is to have the bottom cavity in contact with the oxide, like on Fig 7b) what would isolate the bottom gate.

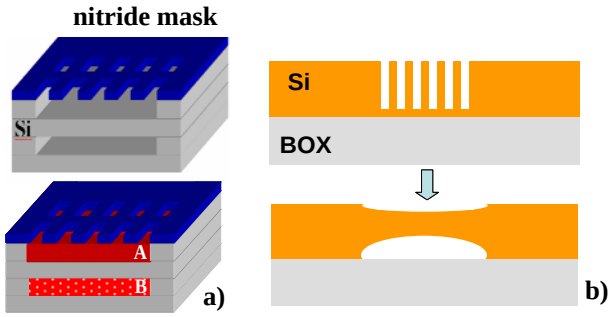

Figure 7: a) Filling of independent autoaligned cavities with different materials (A and B). b) One of the morphologies obtained for a mask-less approach simulated on SOI [3].

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4 CONCLUSION

3D nanostructuration of silicon through hard mask engineering and high temperature annealing (HME-HTA) in hydrogen ambiance with a nitride-capped approach was reported and compared to a mask-less approach. Some of the main technological characteristics and the future potential of this 3D technique have been discussed.

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