Fabrication and Integration of Nanobolometer Sensors on a MEMs Process

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ABSTRACT

In this work, we combine electron beam lithography (EBL) with conventional microscale metal deposition and etch process technologies, to create bolometer devices with nanoscale feature critical dimensions (CDs). We report the creation of titanium (Ti) bolometer devices with 70 nm minimum feature CDs, and total bolometer film thicknesses ranging between 60 nm and 150 nm. Our new nanobolometer devices are integrated with conventional CMOS/MEMs fabrication technologies, creating thermally isolated sensors with nanoscale feature sizes on a 0.5 μm CMOS base process. We also present temperature coefficient of resistance (TCR) data for the new devices, and show a nanobolometer TCR performance of 0.22%/K at 70 nm CDs, comparable to microscale bolometer devices.

Keywords: nanobolometer, nanolithography, sensor, etch, MEMs

1 INTRODUCTION

Uncooled bolometer devices have advantages such as lower cost, better reliability performance and portability, when compared with cryogenically cooled sensors. However, uncooled bolometer detectors have drawbacks, such as low detectivity due to self-heating under constant bias [1], thermal noise, and sensitivity of the sensor material to the fabrication process [2]. To produce highly sensitive uncooled infrared (IR) bolometers, the development of devices that use sensor elements made from high-TCR and low-noise materials is important. In the production of uncooled IR bolometer devices, trade-offs are required between sensor design criteria, choice of bolometric sensor material, and the best device performance deliverable by the wafer fabrication process.

Materials commonly used as bolometer sensor films include vanadium oxides [3]-[6], metals and semiconductors. Vanadium oxide is used primarily to achieve a sufficiently high sensor TCR performance for use in IR sensing applications. However, the deposition and processing conditions for vanadium oxide films are narrowly defined, and they generally require annealing at moderate to high temperatures. Vanadium oxide is also difficult to integrate with mainstream CMOS/mixed-signal wafer fabrication, due to contamination concerns.

Semiconductor films, such as amorphous polysilicon, are compatible with CMOS and mixed-signal fabrication technologies [7], but usually require high temperature annealing. Metal films, such as platinum (Pt) and Ti, are readily compatible with mainstream fabrication processes, [1], [8]-[11]. However, Pt and Ti are susceptible to changes in material and electrical characteristics (including TCR) through the bolometer fabrication flow.

Serpentine sensor element designs, with microscale feature CDs, have been used to increase the effective thermal resistance of the bolometer for a given pixel area. The serpentine structure raises the length-to-width ratio of the sensor resistor, and device sensitivity can be increased through the increase of this ratio. Bolometer IR detectors are also typically designed for high thermal isolation, as this makes them more receptive to small differences in environmental temperature. Surface micromachining [12]-[16], or bulk micromachining [17]-[18] techniques have been used in microscale bolometer fabrication, to create thermal-isolating cavities beneath the sensor areas.

In our work, we explored the trade-offs between sensor design, bolometeric material, and the impact of the fabrication process flow on bolometer TCR performance, at nanoscale sensor element CDs. We used Ti bolometric sensor films ranging in thickness from 60 nm to 150 nm, and MEMs-based silicon bulk micromachining (SBM), to create thermal-isolating cavities beneath the sensor pixels. Ti and SBM process options were chosen because of their compatibility with CMOS, mixed-signal and MEMs wafer fabrication processing.

Fig. 1 shows a schematic of our CMOS/MEMs-integrated nanobolometer process scheme. We incorporated serpentine bolometer sensor elements within our pixel design, to increase the length-to-width ratio of the sensor resistors. Using EBL, we further maximised the length-to-width ratio of the resistor, by creating bolometer devices with sensor element minimum CDs ranging between 350 nm and 70 nm. TCR performance was maintained at nanoscale CDs, and we report TCR values of 0.22%/K at 70 nm CDs. We inserted our nanobolometer fabrication module within the backend of a 0.5 μm CMOS fabrication flow, preventing exposure of the bolometeric layer to medium or high temperature process steps.

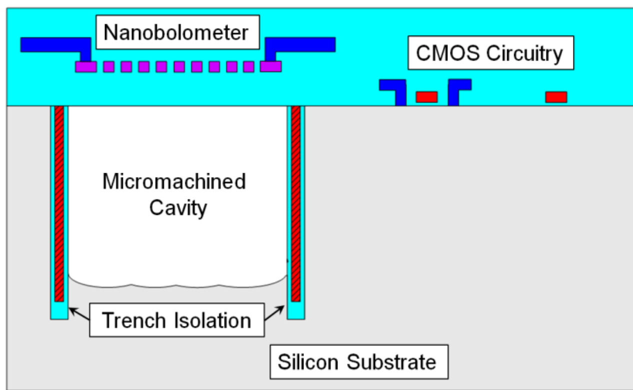

Fig. 1: CMOS/MEMs-integrated nanobolometer process scheme.

2 EXPERIMENTAL METHOD

We used 200 mm substrates running on a 0.5 μm CMOS base process. Prior to CMOS and nanobolometer processing, we pre-defined 50 μm deep silicon trenches in our wafers, and then filled the trenches with a SiO_2 sidewall liner layer and a polysilicon fill layer.

2.1 Nanoscale Resist Features

We used a JEOL 6000FS EBL tool (spot-beam, vector scan), ZEP-520 positive EBL resist, and ZED-N50 resist developer to create our nanoscale bolometer resist features. Resist thickness, exposure and develop processing parameter set points were optimised through a designed experimental matrix. We used post-develop resist thickness, profile and CD data, and post-etch profile and CD data, across local and global topographies, to site our final nanolithography process. We set our final resist spin thickness at 120 nm (as spun on planar substrates), EBL exposure at 100 μC, and resist develop time at 30 seconds. Fig. 2 shows a planar CDSEM image of a nanobolometer serpentine resist feature patterned using our final nanolithography process. The resist features shown have 60 nm minimum CDs.

2.2 Nanoscale Etched Features

Ti bolometer layers ranging from between 60 nm and 150 nm in thickness were deposited on a 1.5 μm thick SiO_2 layer. After EBL resist patterning, the Ti layers were then etched in a LAM Research 9600 plasma etch chamber using Cl_2/BCl_3-based etch chemistries [19]. The plasma nanoscale etch set points were determined through a designed experimental matrix. Our final Ti etch process was determined from analysing responses of Ti, resist and SiO_2 etch rates, and feature profile and CDs, to variations in etch process parameter set points. Following Ti etch, residual resist was then removed using H_2O/O_2 plasma etch chemistries, and polymer residues were removed using a solvent wet strip process. Fig. 3 shows a planar CDSEM image of a Ti nanobolometer serpentine etched feature, defined using our final nanoscale etch process. The etched features shown have 70 nm minimum CDs. The inset in Fig. 3 shows a TEM micrograph cross-section through a Ti nanobolometer meander. The image shows well-defined Ti features, 65nm layer thickness, with 70 nm minimum CDs and 60 nm separation between dense features.

The meander structure layouts were modified (positively biased) to create wider features at the extremes of the serpentine layouts on the nanoscale devices. The pattern biasing was carried out to prevent etch microloading adversely affecting isolated and semi-isolated structure definition [20]. The biasing of the meander layouts can be seen at the top part of the CDSEM images shown in Fig. 2 and Fig. 3.

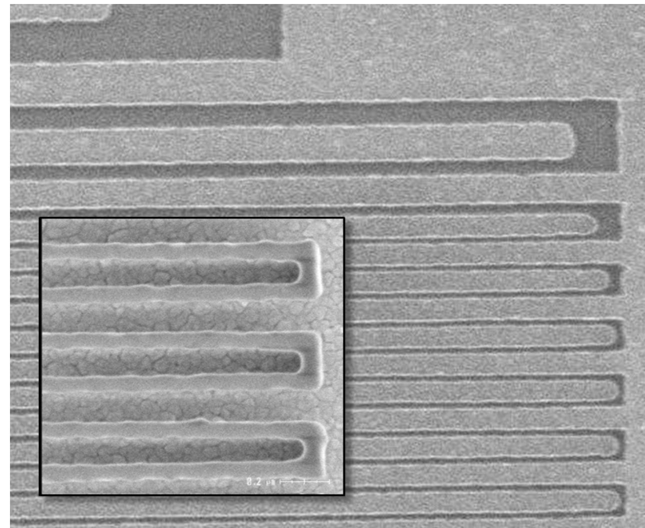

Fig. 2: CDSEM images, of an EBL-defined nanobolometer serpentine resist feature with 60 nm minimum CDs.

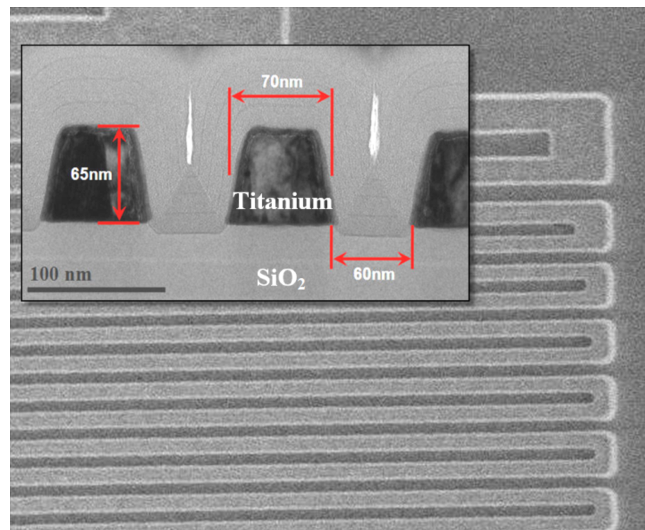

Fig. 3: CDSEM image of an etched nanobolometer serpentine Ti feature with 70 nm minimum CDs. Inset shows a TEM micrograph section through the 70 nm lines.

2.3 Bulk Silicon Cavity Release

The etch-defined nanobolometer structures were capped with passivating dielectric layers and then processed through an SBM fabrication module, to release the final sensor structures from the bulk silicon substrates. The cavity silicon release etch was done on a Xactix xenon diflouride ($XeFe_2$) etch tool. The cavity release process creates a 40 μm deep cavity beneath the sensor platform, providing thermal isolation from the bulk substrate. The pre-defined trenches contain a SiO_2 sidewall liner. The $XeFe_2$ etch process has a high selectivity to the SiO_2 trench layer, and the liner serves as a lateral etch-stop for the silicon cavity etch. The trenches therefore define the lateral boundary for the silicon cavities beneath the sensor pixels. Fig. 4 shows an optical image, planar view, of a fully fabricated nanobolometer pixel, with 70 nm minimum CDs, post-silicon cavity release processing, with the cavity boundary trench visible around the pixel perimeter.

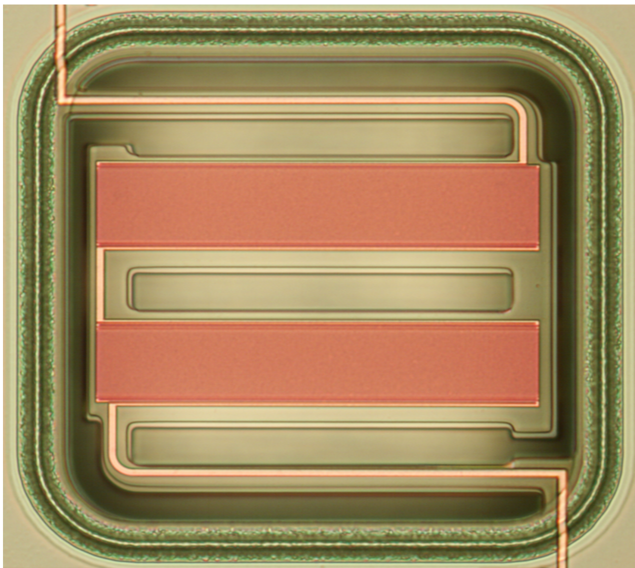

Fig. 4: Optical image, planar view, of a sensor pixel, with 70 nm minimum CDs, after silicon cavity release.

3 RESULTS

3.1 TCR MEASUREMENTS

We used 4-point probe measurements to investigate the TCR performance of the released nanobolometer pixels. Forced current was limited during measurement, to prevent Joule/self- heating in the devices [21]. The device TCR was measured by controlling temperature of the substrate, and measuring resistances at 298K and 373K. The impact of sensor element line width on TCR was also investigated. A range of devices were fabricated, with minimum sensor element CDs ranging from 350 nm to 70 nm, while maintaining the same pixel size and sensor element layout area across all devices.

Fig. 5 shows a graph of the dependence of nanobolometer device TCR on minimum sensor element CD, using the same sensor element layout area on all devices. Fig. 5 shows the TCR reducing as the minimum sensor element CD shrinks. A similar TCR dependence on CD has been previously reported for small-geometry metal interconnects [22]. In the absence of significant self-heating in the devices, the observed TCR and CD dependence can be attributed to surface and grain boundaries scattering processes, as the mean free path of the charge carriers become comparable to the dimensions of the etched nanobolometer features.

The TCR performance of our nanobolometer devices was maintained at 0.22 %/K, at 70 nm sensor element CDs. The sensor TCR values we report are comparable to fabricated microscale bolometer devices referenced earlier in this paper. Our new nanobolometer devices may be suitable for use in high-resolution IR sensing and gas detection applications.

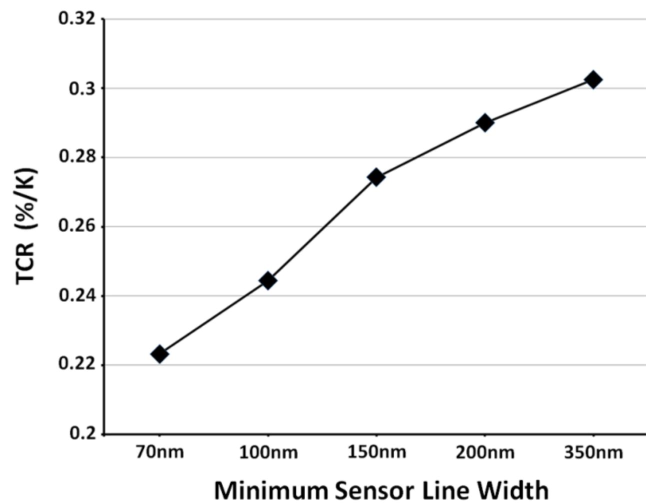

Fig. 5: Graph of 80 nm thick Ti bolometer TCR vs. minimum sensor line width. Temperature delta was taken between 293K and 373K.

4 CONCLUSIONS

We have shown experimentally that EBL and microscale plasma etch technologies can be used to create Ti bolometer sensor elements with nanoscale CDs. We have fabricated devices with Ti sensor layer thicknesses ranging from between 60 nm and 150 nm, and with minimum sensor element CDs down to 70 nm.

Our nanobolometer devices were integrated with a 0.5 μm CMOS process node and a MEMs-based SBM process module, illustrating the flexibility of the new sensor process. Our new devices delivered a TCR performance of 0.22 %/K at nanoscale sensor element CDs, comparable to many microscale bolometer devices. Possible uses for the nanobolometer devices we report include high-resolution IR sensing and gas detection applications.

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