Thermal Cycling of Buried Damascene Copper Interconnect Lines by Joule Heating*

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ABSTRACT

We report tests to failure of 300-nm-wide damascene copper interconnect lines in silicon oxide dielectric, under high amplitude, low frequency alternating current. The cyclic minimum and maximum resistances were obtained from the measured voltage and current waveforms, and remained essentially constant over the lifetime tests. In the lines tested to failure under voltage control at the highest current levels, observed features of the remaining copper deposits seemed to indicate repeated melting over multiple cycles of current. The lifetimes, plotted against temperature, formed a nearly straight line on a semi-log plot, even though the failures, particularly those run under voltage control, became considerably less catastrophic for the longer lifetimes. Understanding the individual and combined effects of the temperature, current, and thermomechanical stresses will open up the possibilities for utilizing these electrical tests in systematic assessments of interconnect reliability and quality control.

Keywords: alternating current, fatigue, stress, temperature, voids

1 INTRODUCTION

Measurements of the lifetime-to-failure of nanoscale structures under relevant stresses allow the reliability of such structures to be quantified. Although extraction and testing of well established specimens, such as microtensile or instrumented indentation, is extremely challenging for nanoscale material features, nanoscale structures that are accessible electrically can often be stressed thermomechanically, by Joule heating, as well as by the "electron wind" that occurs at high current densities and is responsible for electromigration [1]. Stressing by electrical means may offer advantages over other means of reliability assessment, such as mechanical probing, for certain types of nanoscale structures, such as buried features.

Interconnect structures in advanced ULSI (ultra large scale integration) devices are leading-edge nanoscale structures. The smallest line widths are now less than 100 nm, and are buried as many as ten layers deep in the damascene structure. Reliability challenges for the near term include accounting for the effect of surrounding the copper lines with mechanically soft dielectric layers, or perhaps even air, and for the possibility of voids in the copper lines.

Several recent papers describe stressing of films or lines of metal conductors by use of thermomechanical stresses from Joule heating, *e.g.*, [2]. For certain cases of material and geometry, microstructural evidence of mechanical deformation, in particular, dislocations, has been reported [3]. Again for particular cases, the plot of cyclic temperature *vs* lifetime has been found to be similar to the S-N curve for mechanical fatigue, which allowed the extraction from the electrical test data of a fatigue strength that approximated the ultimate tensile strength [4].

A previous report compared the general failure behavior of 300 nm lines and vias in oxide and low-k dielectrics under high amplitude alternating current [5]. Here, additional details of the electrical behavior and SEM (scanning electron microscopy) images of the failure sites are presented. The main benefit of the SEM analyses presented here is to show the type of observations that can be made. Many more experiments will be needed before the sort of observations shown here can be related with a specifiable level of confidence to particular failure modes.

2 EXPERIMENTS

We have applied high amplitude, low frequency (100 Hz here) alternating current to 300 nm damascene copper interconnect lines. A substantial set of lifetime data under current control has been accumulated [5]. In these tests the voltage waveform contains higher harmonics that increase with the imposed current, and the failures are usually so catastrophic that failure investigation by microscopy is uninformative because the details have been obliterated.

Recently we have implemented some new experimental capabilities: operation under voltage control, with adjustment of the voltage waveform to (nearly) eliminate higher harmonics in the power waveform, so that the power becomes a sinusoidal function of time; and recording of both the cyclic maximum and the cyclic minimum electrical resistance during the course of the lifetime tests. The dc resistance is obtained as previously by interrupting the high amplitude alternating current and measuring the resistance at low, static values of current. We have also begun to examine this set of failed lines using SEM and EBSD (electron backscatter diffraction).

2.1 Specimens

Two-level damascene structures were obtained from a commercial source. Here we report tests of M1, the first copper level above the silicon substrate. The lines tested were electrodeposited copper, typical of recent electronics

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industry practice; their nominal dimensions were 300 nm wide, 500 nm deep, and 400 µm long. “Shield lines”, not electrically connected to the test lines, ran parallel to the test lines on both sides. The dielectric was SiO_2.

2.2 Electrical Measurements

The cyclic minimum and maximum resistances were obtained from the measured voltage and current waveforms by fitting each using a discrete fourier transform and then applying a low-pass Weiner filter [6]. The maximum resistance was obtained directly from the fitted waveforms, at the maxima of current and voltage. L’Hôpital’s rule was applied to obtain the minimum resistance, at the zero-crossing of the current and the voltage. The cyclic extrema of temperature were deduced from these resistance values [7].

The power waveform was also analyzed using the discrete fourier transform. The instantaneous power was available as the product of the instantaneous current and voltage values. Under voltage control at frequency f_v, the fundamental frequency of the power ias $2f_v$, and the lowest harmonic was at $4f_v$. Under current control without waveform adjustment, the power amplitude at $4f_v$ sometimes reached 20 % of the fundamental amplitude. The straightforward waveform adjustment that we have implemented reduced the second harmonic of the power to less than 1 % of the fundamental. The purpose of maintaining a single frequency in the power waveform was to impose heat generation at a single frequency. This would greatly simplify the use of closed form solutions for heat conduction, such as those found in Carslaw and Jaeger [8]. The prospective use of the present ac measurements for thermal properties is beyond the scope of this paper.

2.3 SEM Examination

Removal of the upper dielectric layers was necessary in order to examine the failed lines by SEM. This was accomplished by etching the tested specimens in a dilute hydrofluoric acid solution for 4 to 20 minutes, depending on the thickness of the dielectric. Both imaging, for general appearance and topography, and EBSD, to locate grain boundaries and determine grain orientations, were performed in the SEM.

3 RESULTS

The maximum cyclic resistance depended linearly on the maximum cyclic power. By deducing the maximum cyclic temperature from the maximum cyclic resistance [7], we found that the thermal resistance of these lines to ambient was about 700 ºC/W. Typically the three recorded resistances, namely, the cyclic extrema and the dc value, remained nearly constant throughout the lifetime of these lines (Fig. 1). As indicated in the figure, the cyclic minimum resistance in this test is approximately equal to the dc resistance, indicating that the copper line cooled almost to ambient temperature during each power cycle. This behavior was typical for imposed currents at 100 Hz. Occasionally the cyclic maximum resistance increased by a few ohms just before failure, but this was difficult to detect consistently since the resistance measurements were made only every 30 seconds. The lifetimes, plotted against temperature, formed a nearly straight line on a semi-log plot (Fig. 2), even though the failures, particularly those run under voltage control, become considerably less catastrophic for the long lifetimes. The current-control and voltage-control failure trends cannot be distinguished in the presence of the scatter in the data, even though the power waveforms are different in these two situations.

Our attempts to examine the failure sites of tests run under current control have been frustrated by the catastrophic nature of the failures: we find only what looks like the aftermath of a small explosion. These failures occur predominantly near, but not at, the ends of the test lines (Fig. 3). The failure sites of tests run under voltage control are not as catastrophic (Fig. 4).

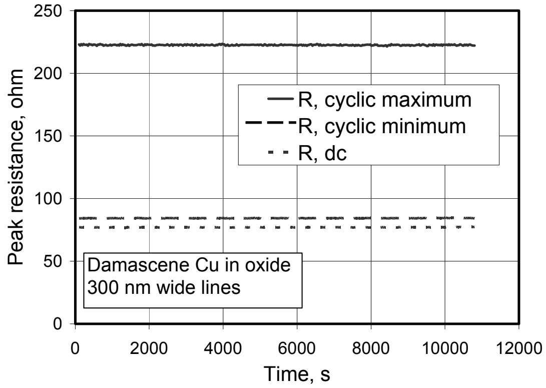

Figure 1. Cyclic maximum, cyclic minimum, and dc resistances plotted against time during a test.

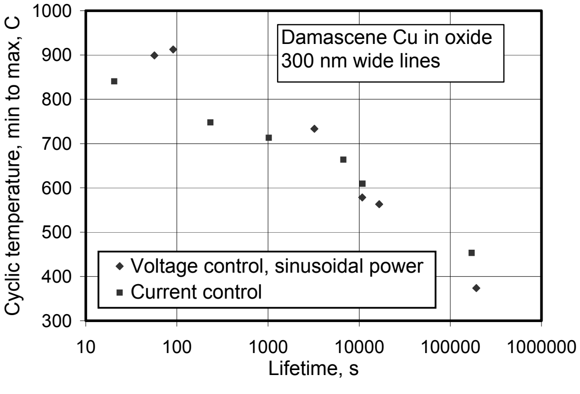

Figure 2. Lifetime plotted against cyclic temperature excursion for a series of tests.

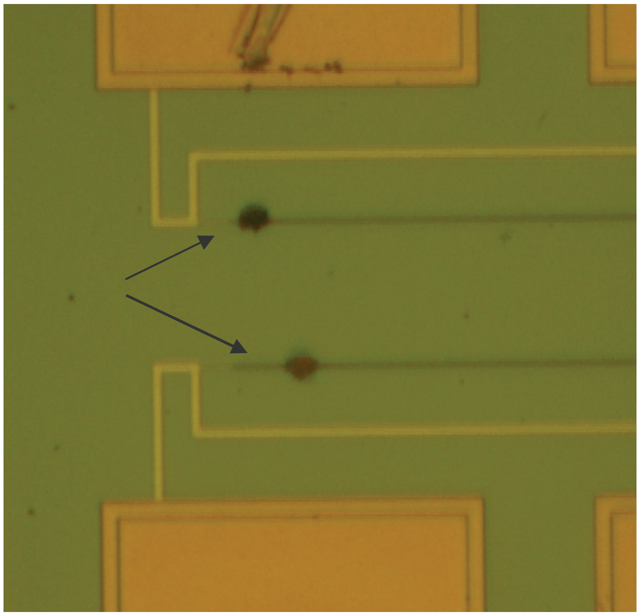

Figure 3. Optical micrograph showing two failed lines. These failures occurred under current control with cyclic temperatures of 455 ºC (lower line) and 555 ºC (upper line). The large copper structures at the top and bottom of the image are contact pads. The buried test line appears dark, rather than copper-colored. The failure sites are indicated by arrows.

SEM and EBSD observations of lines failed under different conditions are shown in Figs. 5-8.

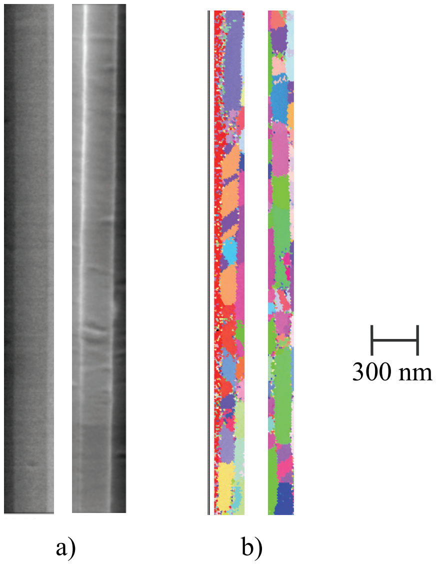

Figure 5. a) SEM images comparing untested line (left) and line tested to failure (734 s at ΔT = 786 ºC) (right); specimen tilted 70 º to enhance topography. b) EBSD images from the same lines; colors represent crystal orientation, used to distinguish grains.

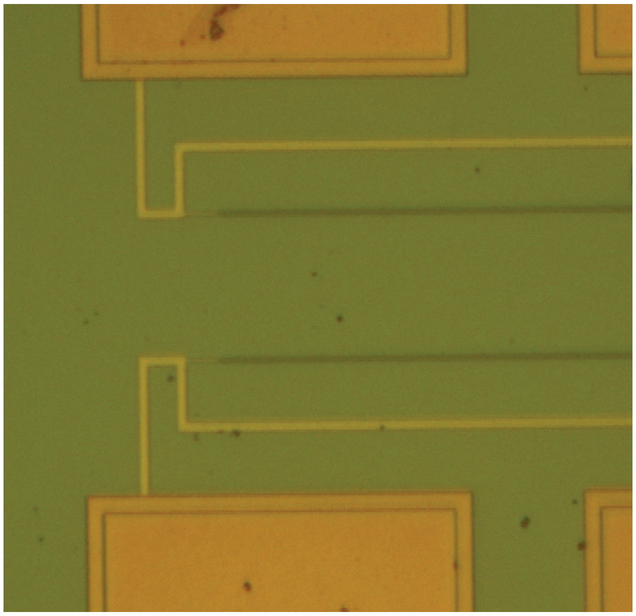

Figure 4. Failures under voltage control with cyclic temperatures of 545 ºC(lower line) and 618 ºC (upper line). Again, the large copper structures at the top and bottom of the image are contact pads, and the buried test line appears dark, rather than copper-colored. The failure regions are not visible in this optical micrograph.

In a set of lines tested under current control at a cyclic temperature amplitude of 786 ºC, we observed a slight increase in topography (Fig. 5a). Observation of multiple EBSD images, such as shown in Fig. 5b, indicates a slight increase in grain length along the lines. Averages of samples of over 40 grains gave an increase in grain length from 0.67 to 0.91 μm. A tendency for the grain boundaries to become more perpendicular to the line axis was also seen.

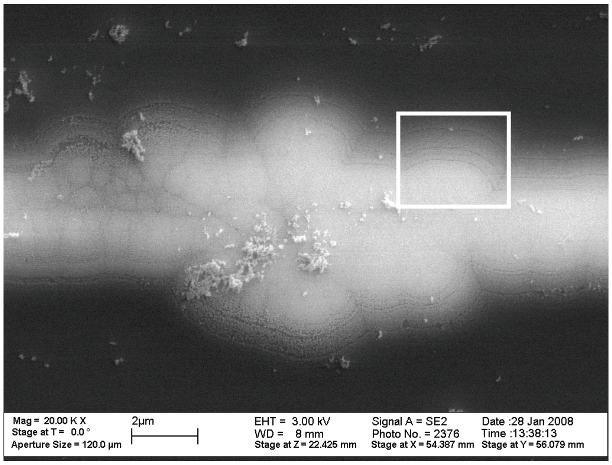

Figure 6. SEM image of failure site showing deposit of melted copper (large bright region in center). The region in the white box is shown in Fig. 7.

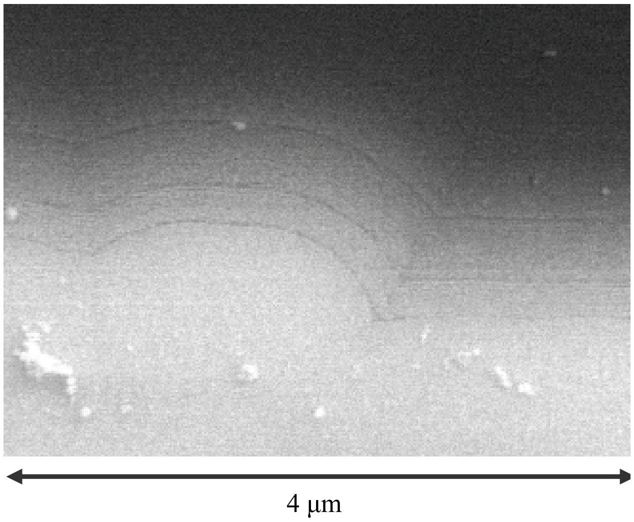

Figure 7. Section of SEM micrograph of failed line shown in part a of this figure, expanded to show features indicative of repeated melting.

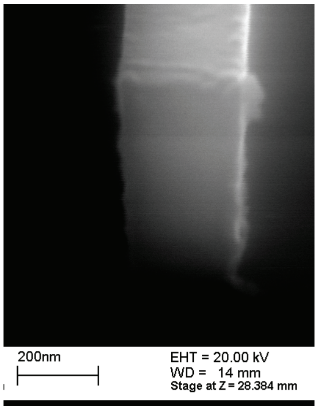

Figure 8. SEM image of 300 nm wide damascene copper line tested under ac to failure under voltage control with a cyclic temperature of 733 ºC, and a lifetime of 3220 s. Note the very "square" failure surface, nearly perpendicular to the line axis.

In the lines tested under voltage control at the highest current levels, copper deposits near the center of the length of the lines and wider than the original damascene lines are found (Fig. 6,7). These deposits appear to be the result of melting, and show features that seem to indicate that the copper was melted repeatedly over multiple cycles of current. Lines tested under voltage control at lesser current values showed very abrupt rectangular failures, almost as if the line had been cut in a controlled fashion (Fig. 8).

4 DISCUSSION

The smooth trend of lifetimes with cyclic temperature shown in Fig. 2 suggests similar failure mechanisms at both the longest lifetimes tested, over 100,000 s, meaning over 20 million heating-cooling cycles of 400 ºC, and at the shortest lifetimes tested, around 10 s, producing only a few thousand temperature cycles that reach 900 ºC on average.

These initial microscopic observations of electrically-driven open-circuit failures suggest that failure occurs when a grain boundary or a void perpendicular to the line gradually opens up to become crack-like. This would reduce the local cross-section of copper carrying the current, leading to a local thermal runaway under current control, or to an eventual, less catastrophic open-circuit failure under voltage control. Signs of local melting at failure sites have been observed for failures under both current control and voltage control.

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