Advances in electrolytic plating technologies for plating nano & micro structures

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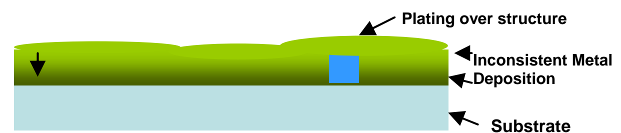
Abstract

Electroless and Electrolytic plating has had to keep up with the demands in developing new technologies to meet the needs of filling nano and micro structures. Requirements have been for plating angstrom thin layers with an equal deposition over an entire 300 mm wafer, filling high aspect ratio structures with deep side walls, with out voids and plating up varying width structures at the same time Digital Matrix primary function as a company is to manufacture high-speed, high-precision electrolytic plating equipment. With the demands and requests presented to them, they have been frequently asked to solve the plating tribulations created by various aspects of the MEMS/NEMS industries. A few of the more significant technologies performed are: • Digital Matrix process and system can control the plated deposition over the entire wafer surface with a consistent TTV. (Total Thickness Variation) • The process developed by DM allows the plating up of varying width and height structures to grow at the same rate, eliminating the need to slurry away the excess and lose valuable time and precious metals. • Digital Matrix has developed a bump plating process that can over-plate posts/pillars straight up over the Photo Resist or mask, 20 μms with out the mushroom or muffin affect. Larger bumps can be created with a slight mushrooming formation. This technology is being used to replace the need for solder bumps. • Deep posts and side-walls can be plated, filling in the corners and with no trapped voids. • Exact height plating can be achieved, eliminating the need to slurry excess over-plating. • Angles created in Photo Resist can be plated into the deep corners and acute angled side walls without voids.
Keywords: electrolytic, plating, high-aspect-ratio, vias

The demands put on the MEMS and Nano industries have overwhelmed all aspects of research and development, especially electroplating. When we feel we have made it the smallest possible, we have to make it even smaller, and we have to manufacture trillions of these items in record time, as cheap as possible. Every phase of producing a MEMS or Nano part needs to comply with numerous other demands imposed in manufacturing the substrate and each must meld perfectly to complete the final product…within angstroms.

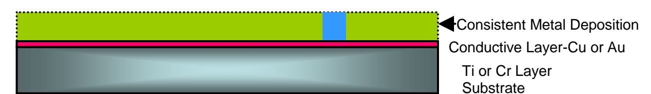
There are many phases that go into the preparation of a wafer before plating and if every phase is performed within spec, advanced plating techniques have the capabilities of out performing previously impossible tasks.

Wafer plating has generally relied on Electroless plating (Illustration 1) to layer several metals uniformly, but this requires slurry stages to remove excess and over-plated areas. There is limited control of the TTV (total thickness variation) and deposition. It is a slow and arduous process with a limit of 100 micron thickness and real concern of stress. The chemicals weaken over a period of time and are tossed for recycling, a very expensive and environmentally wasteful procedure. As the chemical composition changes, the properties of the metal deposition layer drift. This leads to a non uniform and out of specification result. Properties such as hardness can change dramatically.



(Illustration 1)

Electrolytic plating, (Illustration 2) also known as High-Speed Plating, has recently become the preferred method because of its capabilities of out performing the Electroless process. The absolute control of plating parameters can be within 1 to 5% of the specifications and can be controlled in angstroms with an excellent thickness uniformity (low TTV). There is no need to slurry excess areas and there is virtually no limit to the height of the plated area. Electrolytic plating can be up to ten times faster than the Electroless process and chemicals are NOT disposed of but maintained recycled within the system. Hardness and other properties are much more consistent and easily maintained. Thickness can range from <0.001 micron to 10,000 microns.



(Illustration 2)

Most metals used in the Electroless process can also be deposited electrolytically, and various formulas are available to meet a wide range of requirements. Digital Matrix has developed their own special formulations to maximize results and have focused on the elimination of organics that generally cause stress.

Nickel Cobalt

NiCo, one of the preferred for its high hardness. Typically NiCo high-speed NiCo plating is plagued with such as internal stress, tensile and brittle structures. It also generally requires special organics additives and constant metered replenishments of Cobalt Sulfamate.

Digital Matrix has reduced the stress from 150,000 psi to 0 psi and created a hardness of 680 HV by maintaining the process parameters such as pH (3.8 to 4.1), Stag Factor (1.6-1.9) and Boric concentration (25 to 35%), temperature (60ºC to 65 ºC) and current density from 0.1A/dm2 to 5.5A/dm2. Co-ion concentration is 5-6 g/L and Ni-ion concentration is 130-140 g/L. DM programs 3 to 9 gradual plating ramp steps from low DC and RPP (reverse pulse plating) current density to high DC and RPP current density.

Copper & Copper Alloys

In the familiar Cu process, organics such as Cuprax, Acid Cu Sulphate, Cyanide and Pyrophosphate solutions are used. Cuprax and Cyanide are used for heavy Cu deposits that are smooth and fine grained. Cuprax Cu used 160 to 120 g/L of High-Efficiency Cuprax Salts and Cyanide Cu uses 5 g/L Sodium & Potassium-Cyanide and Sodium-Sulphite to keep the anodes clean.

The Digital Matrix Cu Pyrophosphate formula requires high-speed, rotating head, electrolytic plating. This very stable process uses Cu-Phosphate 70-90 g/L, Potassium-Pyrophosphate 220-240 g/L and Ammonia Liquor 3-5 ml/L.

The CuAlloy solution has a pH range from 1.8 to 3.8 and the average current density is 0.1A/dm2 to 3.0A/dm2. Temperatures can range from 20ºC to 50ºC. Plating times can vary from 2 to 4 hours for 100 µms and 1 to 2 hours for 50 µms achieving a +/- 1 µm TTV. DM recommends Copper Sulphate 200-280 g/L, Sulphuric Acid 20-50 g/L and additives; Brightener and Refiner.

The results are stress free with pre and post plating, and TTV within +/-1 to 5% and a perfect adhesion to Au and other Cu layers. With an achievable hardness of 250 Vicors, the mechanical strength of a Cu film becomes non-destructive and creates a perfect electrical resistivity of the plated area.

Digital Matrix standard Cu Acid solution can withstand very high plating speeds and meet hardness requirements of approximately 250 Vicors. It is a more stable process than a cyanide based solution. DM's formula uses a Cu-ion concentration of 80 to 90 g/L, Cu Sulfamate concentration of 260 to 270 g/L, Sulfuric Acid (10 to 30 ml/L), Specific gravity: 1.167 to 1.17, with a stag factor of 1.4 to 1.9 and a temperature of 23ºC to 25ºC. Current density is 0.001A/dm2 to 0.008 A/dm2

Other Benefits of Electrolytic plating with DM Equipment

Other benefits of Electrolytic High-Speed Plating are

- Plate to exact height of the structure +/- 1 to 3µm
- Plate without voids and defects
- Plate in corners and sidewalls of high aspect posts
- Smooth back finish with a mirror finish
- No tensile or brittle structures
- Plate 20µm above photo-resist -straight up
- Plate exact thickness thru diameter: +/-1 to 3µm
- Adjust the distance from the Cathode to Anode
- Plate in a fraction of the time of your previous cycle

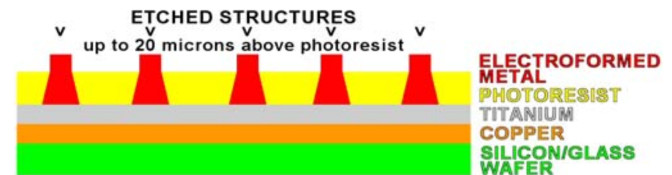
Plating On Aluminum:

As Silicon wafers become harder to purchase, labs are looking at alternative substrate materials to plate to, such as Aluminum. Digital Matrix has formulated a process that makes plating to Al easier and within the required specifications. With the use of special adhesion layers, such as Ti, Cr & Zn, additional layers, such as Ni, Cu, Au, can be plated to the Al. Unlike traditional Electroless processes, DM has a process that can plate in excess of over 300 microns

Plating Structures:

Digital Matrix has used their High-Speed Electrolytic plating systems to achieve many various results that have helped to revolutionize the Nano and MEMS industry. With the ability to plate with exact and precise properties, the plating equipment and metal plating formulas have opened up new techniques, allowing a more eco friendly and less expensive method to achieve results once thought un-obtainable.

Illustration 3 demonstrates an even more unique Digital Matrix proprietary process that offers multiple opportunities when using an electrolytic process that most would not have considered in the past. The resulting structure can be a 3-D part that can also be removed from the wafer as a micro part. The structure etched into the photo-resist can be prismatic or octagonal in shape and carry the shape up to 20 microns above the photo-resist, or it can create a bump over the PR without a mushroom affect.

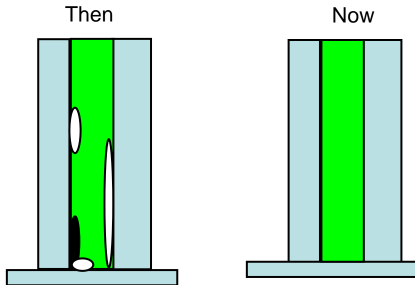


(Illustration 3)

The Bump affect has been used in various applications, but where it has received the most attention is in the Semiconductor packaging industry. With the environmental concerns to replace lead/tin, it is now possible to plate this in any metal, allowing for a harder bump. DM is capable of plating 20 µms over the top of the PR or mask without mushrooming and can grow 45 to 50 microns over with an ever so slight mushroom affect. These can also be done in Nano bumps and with a closer placement. It is much faster and more reliable than the standard bump process and the

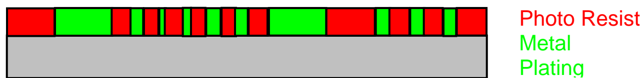
adhesion is excellent when the preparation is performed properly.

Side-wall deposition and Vias have also created challenges to most facilities. As soon as you let someone know you can plate a side-wall or a via, they immediately push to a smaller structure and higher aspect ratio. The challenges have been to remove the hydrogen bubbles that get trapped in the bottom corners and walls. (Illustration 4)



Digital Matrix has a 45° angled, rotating, cathode workholder that spins at an adjustable 60 rpms that will spin out the trapped bubbles, giving strength to the structures for mass production.

Filling structures of varying widths and height on the same wafer would ordinarily cause over-plating on the smaller or narrower structures, while the wider and deeper structures would take longer to fill, often causing a dip or uneven fill. Digital Matrix has developed a program and process to plate at the same rate so that the narrow structures would plate at the same rate as the wider areas. (Illustration 5)



Plating requirements of exact thickness are easily achieved on a DM plating system. With a structure height of 292 microns high it is desirable to plate 292 microns consistently across the entire wafer, we can do this within +/- 1%. This eliminates the need to slurry to remove high edges or center. This potential has been increasingly interesting to those who plate Au or any of the other precious metals. The need to remove and then recover expensive metals is eliminated. The tolerances are also controlled by the vacuum sealed cathode backplate that draws the air from behind the wafer, allowing for more precise results. (Illustration 6)

(Illustration 6) 300 mm vacuum rotating cathode backplate

Plating requirements will always be put to the challenge. It is not enough to work with older processes and technologies to achieve the results required today. What was once the answer, may no longer apply to today's demanding specifications.

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