Multiple Gate Approach - Solution of Scaling & Nano-MOSFETs

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ABSTRACT

In the nm scale, the aggressive scaling of MOSFETs is expected to culminate in dual-gate (DG) architectures on SOI substrates. DG MOSFETs are widely accepted to be the ultimate design that silicon can deliver in terms of on and off currents. So far, the design efforts on these novel structures have concentrated on ideal geometries and doping profiles. The paper describes the evolution of the SOI MOSFET from single-gate structures to multiple gate (double-gate, tri-gate, π-gate, and gate-all-around) structures. Increasing the "effective number of gates" improves the electrostatic control of the channel by the gate and, hence, reduces short-channel effects. Due to the very small dimensions of the devices, one-and two-dimensional confinement effects are observed, which results in the need of developing quantum modeling tools for accurate prediction of the electrical characteristics of the devices. It also includes the effect of silicon thickness, when we are using multiple gates, the effects of different gate potentials on multiple gate MOSFETs, Doping concentration of Source/Drain/Channel region, thickness of SiO_2 layer, and more.

Keywords: MuGFETs, Mobility, Doping.

1 INTRODUCTION

Due to the continuous and aggressive scaling, silicon MOS devices have rushed into the sub-100 nm regime. In the nano-scale regime, main challenges in device design are the suppression of short channel effects and the management of quantum effects. The short channel effects and quantum effects would severely degrade the device performance in the nano-scale MOSFETs. For scaling as projected in the ITRS to take place, the industry must be capable of cost-effectively fabricating MOSFETs with the required characteristics, which includes meeting the $I_{sd,leak}$ and transistor performance, control of SCE, acceptable control of the statistical variability of the MOSFETs parameters, acceptable reliability, etc.

The paper is organized as follows. Section II consist of scaling challenges and its potential solutions, Section III gives details of model used, Section IV, & V includes device simulation and conclusion respectively.

II MOSFET SCALING CHALLENGES & POTENTIAL SOLUTIONS

It turns out that there are numerous difficult challenges that arise as the technology is scaled with succeeding years and that significant technological innovations will need to be implemented in relatively rapid succession to deal with these challenges are:

*2.1 Mobility enhancement***:**

The first difficult challenge with scaling is increasing the I_{dsat} as much as required while holding $I_{sd,leak}$ to acceptable values. The preferred solution is to enhance the mobility beyond that attainable with standard silicon channels by using strained Si, possibly strained SiGe channels. Strained Si channels with enhanced mobility were implemented [1]. Mobility enhancement up to 1.8 times be obtainable for strained Si channels has been reported for nMOSFETs, and even higher for pMOSFETs [2].

2.2 Gate leakage reduction:

The gate leakage is due to direct tunneling of electrons through the gate dielectric, which increases sharply as the gate dielectric equivalent oxide thickness (EOT) is reduced. The ITRS specified maximum allowable gate leakage current density ($J_{g,limit}$) is closely related to the $I_{sd,leak}$. The potential solution being actively pursued by the industry is to use high-k gate material [3]. As a result, for the same EOT, the physical thickness is larger for the high-k dielectric than for silicon dioxide, so the direct tunneling and thus the gate leakage current should be lower for high-k dielectrics.

2.3Performance using metal gate:

As Polysilicon gate depletion increases the equivalent EOT, and hence reduces the value of I_{dsat} that can be attained. As the EOT scales with succeeding years, the influence of polysilicon depletion on EOT becomes proportionately greater, and according to the ITRS forecasts that by 2008, polysilicon depletion needs to be reduced below that attainable with polysilicon electrodes if the performance requirements on I_{dsat} and τ are to be met. Metal gate electrodes, which have virtually no depletion, are being developed as the most likely potential solution [4]. To be able to set V_t to the appropriate value for pMOSFETs, the work function of the metal gate electrode must be near the silicon valence band. For nMOSFETs, the work function must be near the silicon conduction band. It is likely that different metals with appropriate work function for the pMOSFET and nMOSFET, respectively, will be used [5].

2.4 MuGFETs structures:

Even with use of the above technology innovations, effective scaling of classical bulk MOSFETs is expected to become increasingly challenging for 2008 and beyond. Achieving adequate control of SCE for such devices will be difficult. Exceedingly high values of channel doping will be needed to control these effects, and high doping will lead both to reduced mobility and increased band-to-band tunneling leakage current. Furthermore, the total number of

dopant atoms in the channel for such small MOSFETs is relatively small, which leads to large and irreducible statistical variation in the number and placement of the atoms, and hence to unacceptable statistical variation in V_t, and degrades the short channel characteristics and sub-threshold slope through an increase of penetration of the drain electric field lines in the channel region [6-7]. A potential solution is the use of ultra-thin-body fully depleted silicon-on-insulator [8] technology. These have lightly doped channels, and V_t is set by the work function of the gate electrode not by dopant atoms in the channel, so the variation in the number of dopant atoms does not affect V_t [9]. Scalability and control of SCE are significantly enhanced, although reliably controlling the thickness will presumably be a major challenge. To prevent the electric field lines originating at the drain from terminating under the channel region, special multiple-gate structure devices have been reported. MuGFETs have attracted much attention owing to their ability to enhance the electrostatic control of the gate over the channel Thus MuGFETs are very attractive, because of threshold characteristics, higher drive current, better short channel effect, effective control, less drain induced barrier lowering etc.

III MODEL

Fig.1 shows the existing gate configuration for thin-film SOI MOSFETs: 1) single gate; 2) double gate; 3) triple gate; 4) pi gate; 5) omega gate; and 6) GAA configuration. The most familiar is the double gate where the gate is formed around the channel, or the two gates are electrically connected. Other form is to have the two gates be electrically independent and be controlled separately; here the second gate is used to shift threshold voltage of the first gate. The sub-group of triple gates is **π**-gate, and **Ω** gate. In case of **π**-gate, structure gate electrodes extends to some depth in the buried oxide on both sides of device, and gate is in shape of Greek letter **π**; and in case of **Ω** gate, it closely resembles to GAA as its gate almost wraps around the body, having top gate like the conventional UTB-SOI, side walls like FinFETs, and special gate extension under the silicon body. Here, a full quantum-mechanical treatment of electron transfer, in particular of the electron confinement in the direction across the ultra thin channel, and the source -to-drain tunneling in the direction along the channel is must. Indeed the lateral effect provides one of the major limitations for transistor scaling [6-7]. Another major effect is a gradual loss of electrostatic control of the channel potential as the gate length L is decreased. So we address these problems by the self consistent solution of 1D Schrödinger equation and 2D Poisson equation. The simulated structures have a uniform doping concentration in the channel and source/drain regions. Abrupt source and drain junction are used. The simulations are carried out using single charge carrier.

IV DEVICE SIMULATION

Electrical characteristics of devices were simulated (using Multi-gate Nanowire FET on http://nanohub.org [10-11]) for the silicon island having width and thickness of 25 nm, while the gate oxide thickness is 1.5nm. Tungsten is used as gate (work function = 4.63 eV), doping concentration in channel is uniform and equal to 1 x 10^{15} cm^3. Simulation is performed for gate lengths L, of 10, 20, 30, 40, 50 & 60 nm. We have used a width of 25 nm, to prevent the electrical field lines from the drain from terminating on the back of the channel region, because of the bottom part of the **π**, **Ω** and GAA

4.1 Natural length model

It gives a measure of the short channel effect inherent to a particular device structure. The concept of "natural length", λ represents the extension of the electric field lines from the drain in the channel region [12]. A device is said to be free of short channel effects if the gate length is at least 5-8 nm larger than λ. Suzuki et al [13] has given expression for λ and given by

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{4\varepsilon_{Si}t_{ox}}\right)t_{Si}t_{ox}} \quad (1)$$

Where t_{si}, t_{ox} are the silicon and oxide thickness and ε_{Si}, ε_{ox} are the permittives of Si, and SiO_2. In 2007, Lee et.al. Calculated the expression for generalizing the λ concept to all MuGFETs by writing

$$\lambda_n = \sqrt{\frac{\varepsilon_{Si}}{n\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}t_{Si}}{4\varepsilon_{Si}t_{ox}}\right)t_{Si}t_{ox}} \quad (2)$$

Where n is the effective no of gates, whose value is calculated from the dependence of threshold voltage on silicon film thickness, and its value decrease as the no of gates increases from single gate MOSFETs to GAA MOSFETs because of the increasing influence of the gate over the potential in the channel region.

4.2 Back Channel conduction & DIBL model.

As the vertical potential profile underneath a thin-film SOI device is controlled by potential lines originating from the source and drain rather than by the front gate, the potential inside the buried oxide increases linearly with drain bias. This lateral potential coupling from the source and drain causes back-channel conduction and DIBL. Fig. 2(a) & (b) shows the drain-induced barrier lowering effect and the threshold voltage roll-off in fully depleted SOI MOSFETs with different gate structures and different effective gate lengths. The DIBL is defined as the difference in threshold voltage when the drain voltage is increased from 0.1 to 1 V. The threshold voltage roll-off, ΔV_{th}, is defined as the threshold voltage measured at V_{DS} = 0.1V at any gate length minus the threshold voltage at L = 50nm. DIBL is most effectively suppressed by the quadruple-gate structure, but the **Ω** and **π** -gate device comes a close second and third. The reason for less short channel effects in **Ω** & **π** -gate device is that the lower part of the gate sidewalls effectively acts as a back gate through lateral field effect in the buried oxide. Similarly, it can be observed that the threshold voltage roll-off is minimized by the use of the quadruple-gate structure, but the **Ω** & **π** -gate device shows an excellent behavior as well.

4.3 Subthreshold swing Model

From the linear relationship between threshold voltage and film thickness, one can derive the general threshold voltage law for multi-gate devices:

$$V_{thN} = V_{Fb} + 2\phi_f + \frac{qN_A}{C_{ox}} \cdot \frac{t_{Si}}{N} \quad (3)$$

We have used N = 2.0 for a double-gate, N = 2.3 for electrically independent double gate, N = 3.0 for a triple-gate, N = 3.14 for a π-gate, N = 3.4 for an Ω-gate, and n = 4.0 for a GAA. The equivalent gate number N depends on the gate extension depth for **π** -gate devices and the lateral extension depth of the side gate in **Ω**-gate devices. Thus we conclude from Fig. 3, that subthreshold swing degradation is smallest in the GAA, **Ω** & **π** gate.

4.4 Model based on doping concentration

To reduce short channel effects, the substrate doping concentration should be increased; Fig. 4 shows the threshold voltage roll-off, ΔV_{th}, as a function of effective gate length for different gate structures and different doping concentrations. As the doping concentration increases ΔV_{th}, is reduced due to the reduction of sharing charge between the gate and source/drain junction. It is also worth noticing that the sensitivity of the ΔV_{th} to the doping concentration is minimized in the GAA structure compared to the others.

4.5 Model based on Channel Width & Silicon Film Thickness

In the present simulation, the silicon island is assumed to have a rectangular cross section and the gate oxide has a uniform thickness in all devices (It is assumed that there is no gate oxide thinning at the edges of the silicon island.) In thin-film single, double and quadruple-gate devices operating in the subthreshold region most carriers flow through the middle of the film due to the volume inversion. In a triple-gate device, the electric field, from source and drain encroaches on the channel region and tends to induce more inversion charge at the bottom of silicon body as device width is increased. When the back channel subthreshold current becomes important, the subthreshold swing degrades significantly. A triple-gate device behaves like a single-gate device when the channel width becomes large. Fig. 5 shows that the threshold voltage of double-gate and quadruple-gate devices increases when the channel width is increased, while the threshold voltage of the triple, **Ω** & **π** -gate device decreases. Figs. 6 show the DIBL and subthreshold slope as a function of the channel width for different gate structures, L and T_{Si} are both equal to 25 nm and N_A is equal to 1 x 10^{15}cm^{-3}. Both the DIBL and subthreshold slope increase slightly as the channel width increases in double-gate and quadruple-gate devices, but they increase abruptly in the triple, **Ω** & **π** -gate device. The DIBL increases with channel width in the triple, **π** & **Ω**-gate device but still its value is lower than that of the double-gate device for channel widths below 45 nm. The subthreshold slope of the Triple, Pi and Omega -gate device increases with channel width but is lower than the double-gate device. The larger DIBL and subthreshold swing in triple, **Ω** & **π** -gate devices is due to the encroachment of the electric field lines from drain on the back of the channel region. This effect increases with device width. The degradation in the quadruple-gate structure is the smallest and, followed by **Ω** & **π** -gate once again. Even though the use of thin silicon film increases the source and drain resistance [12-14], a small silicon film thickness is required to improve the SCE immunity and subthreshold slope. If the silicon film is ultra thin, energy quantization effects start to appear, which influence the threshold voltage and the I-V characteristics of SOI MOS devices [15-19] Fig. 7 shows the threshold voltage as a function of film thickness with different gate structures. The threshold voltage is almost constant for the quadruple-gate MOSFET but it decreases slightly for the **Ω**, **π** & triple-gate structures. Surprisingly the threshold voltage of the double-gate device decreases when the film thickness is increased.

IV Conclusion

The paper establish the guideline for minimum gate length to avoid short channel effects and excess subthreshold swing degradation for different gate structures and different gate lengths W = T = 25 nm, N_A = 1 x 10^{15} cm^{-3}. In the case of a double-gate device the minimum gate length is 40 nm. In the case of Triple gate is 35nm. Pi-gate 30 nm, while for omega and GAA it is 25nm.

V References

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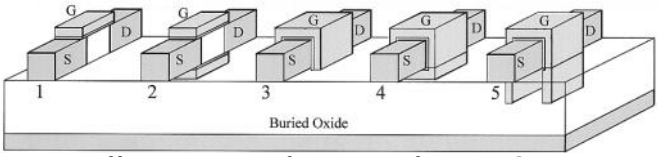
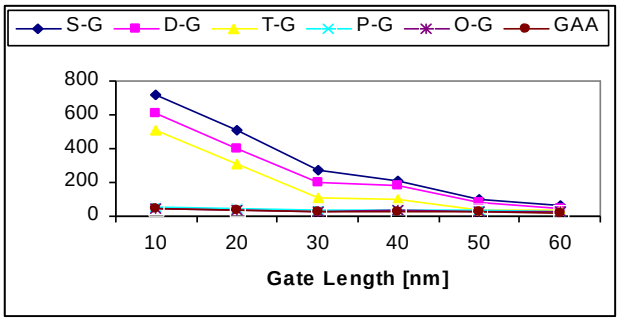
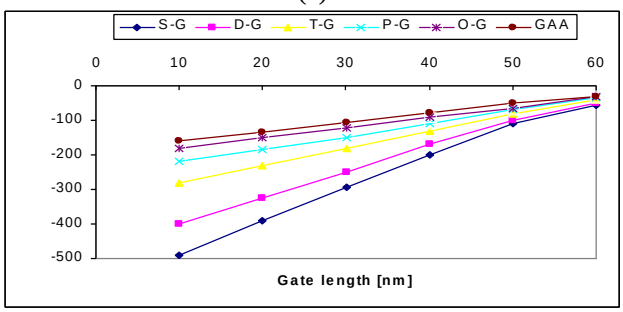


Fig. 1: Different gate configurations for SOI devices: 1) Single gate; 2) Double gate; 3) Triple gate; 4) GAA gate; 5) Pi-gate MOSFET.



(a)



(b)

Fig. 2; DIBL and threshold channel roll-off in fully depleted SOI MOSFETs with different gate structures and different gate lengths W = T_{Si} = 25 nm, N_A = 1 x 10^{15} cm^3.

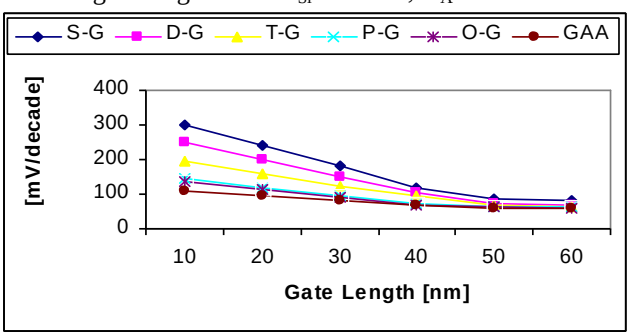


Fig. 3: Subthreshold swing in fully depleted SOI MOSFETs with different gate structures and different gate lengths W = T_{Si} = 25 nm, N_A = 1 x 10^{15} cm^3.

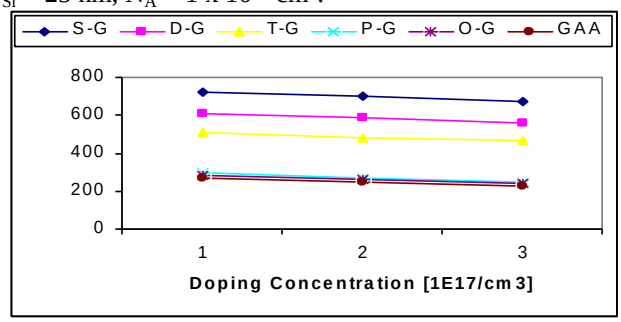


Fig. 4: DIBL in fully depleted SOI MOSFETs with different gate structures and different doping concentrations as a function of gate lengths W = T_{Si} = 25 nm, N_A = 1 x 10^{15} cm^3, 2 x 10^{15} cm^3, and 3 x 10^{15} cm^3

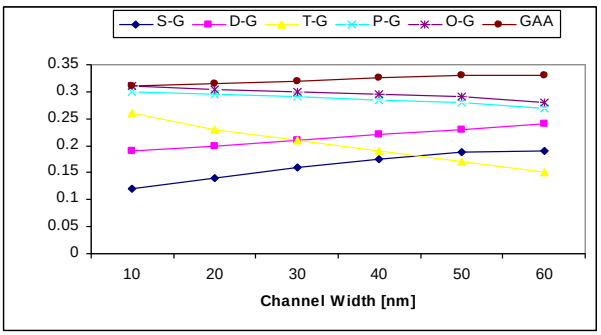


Fig. 5. Threshold voltage in fully depleted SOI MOSFETs with different gate structures and different channel widths W = T_{Si} = 25 nm, N_A = 1 x 10^{15} cm^3

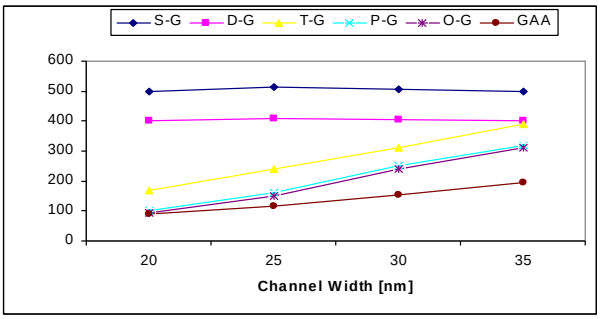


Fig. 6. DIBL in fully depleted SOI MOSFETs with different gate structures and different channel widths W = T_{Si} = 25 nm, N_A = 1 x 10^{15} cm^3

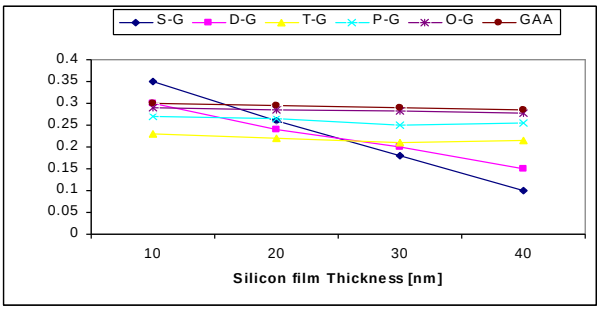


Fig. 7. Threshold voltage in fully depleted SOI MOSFETs with different gate structures and different silicon film thickness L = W = 25 nm, N_A = 1 x 10^{15} cm^3

Remark:

S-G stands for Single gate;
D-G stands for Double gate;
T-G stands for Triple gate;
P-G stands for Pi Gate
O-G stands for Omega Gate
GAA stands for Gate all around MOSFETs.